R8C/1x, 2x Series

R8C/1x, 2x Series Standard Serial I/O Mode Protocol Specification

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1. Abstract

This document defines the R8C/1x, 2x Series Standard Serial I/O Mode Protocol Specification. The boot program stored in the boot ROM area prior to MCU shipment can control the flash memory by communicating with a serial programmer. Standard serial I/O mode 2 or standard serial I/O mode 3 can be selected for communication.

2. Introduction

This document defines the following:

- Boot program
- Initial settings
- Control commands
- Timings

Applicable products:

- Standard serial I/O mode 2
  R8C/1x, 2x Series

- Standard serial I/O mode 3
  R8C/1x, 2x Series (excluding R8C/10, 11, 12, and 13 Groups.)

3. Boot Program

The program in the boot ROM area operates when the MODE pin is set to low and reset is deasserted. This is called a boot program. To enter boot mode, hold the MODE pin low for 30 ms or more before and after reset is deasserted as shown in Figure 4.1.

3.1 Operating Environment

(1) Standard serial I/O mode 2 for R8C/10 to R8C/19, R8C/1A, R8C/1B, and R8C/20 to R8C/29 Groups
CPU clock and count source for communication: External oscillator frequency no division

(2) Standard serial I/O mode 2 for R8C/2A to R8C/2D Groups (96 KB and 128 KB versions)
(a) Boot program Ver.1.00
CPU clock: Typ. 8 MHz generated by the high-speed on-chip oscillator
Count source for communication: External oscillator frequency no division
(b) Versions starting from boot program Ver.2.00
CPU clock and count source for communication: Typ. 7.3728 MHz generated by the high-speed on-chip oscillator

(3) Standard serial I/O mode 2 for R8C/2A to R8C/2D Groups (48 KB and 64 KB versions)
CPU clock and count source for communication: Typ. 7.3728 MHz generated by the high-speed on-chip oscillator

(4) Standard serial I/O mode 2 for R8C/2E and R8C/2F Groups
CPU clock: Typ. 8 MHz generated by the high-speed on-chip oscillator
Count source for communication: External oscillator frequency no division

(5) Standard serial I/O mode 2 for R8C/2G, R8C/2H, 8C/2J, R8C/2K, and R8C/2L Groups
CPU clock and count source for communication: Typ. 7.3728 MHz generated by the high-speed on-chip oscillator

(6) Standard Serial I/O Mode 3
CPU clock and count source for communication: Typ. 8 MHz generated by the high-speed on-chip oscillator

Communication may not be available due to frequency fluctuations of the high-speed on-chip oscillator depending on usage conditions. Refer to the hardware user's manual or Renesas Electronics website for high-speed on-chip oscillator electrical characteristics. Refer to the hardware user's manual for Electrical Characteristics of the erase and program voltage.
Careful evaluation on the user system is recommended when communicating or reprogramming.

3.2 Boot Program Content

(1) Initial settings
(2) Initial communication with a serial programmer
(3) Control commands
Flash control commands (program, erase, and read)
Various setting commands (such as communication speed setting and status read)

3.3 Communication with a Serial Programmer

Standard serial I/O mode 2 or standard serial I/O mode 3 can be selected for communication with a serial programmer. Standard serial I/O mode 2 is an asynchronous communication format. Standard serial I/O mode 3 is an asynchronous half duplex communication format. Figure 3.1 shows the Communication Format.

The transfer data format is as follows:
Start bit: 1 bit
Transfer data: 8 bits
Parity bit: Not used
Stop bit: 1 bit

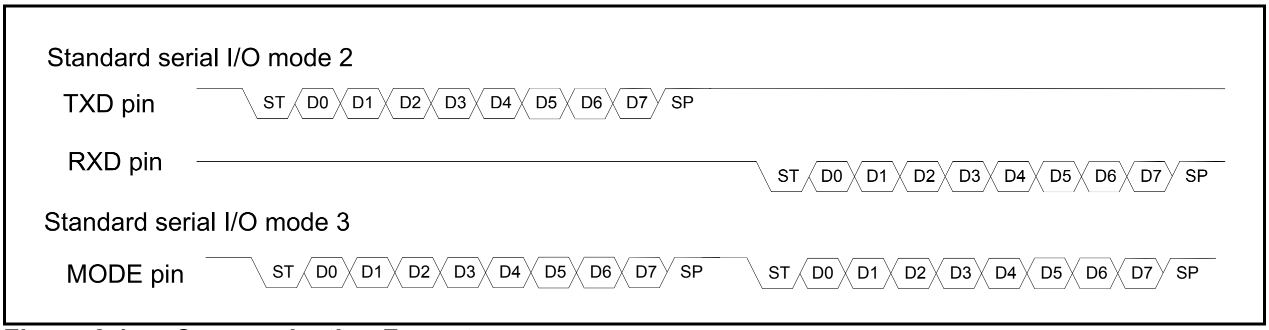
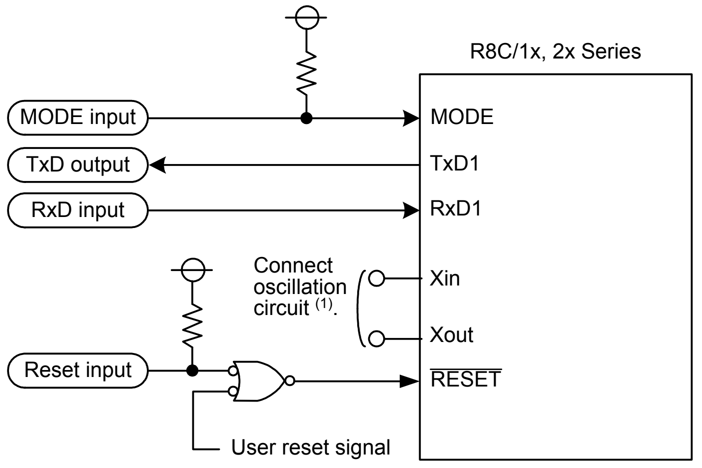


Figure 3.1 Communication Format

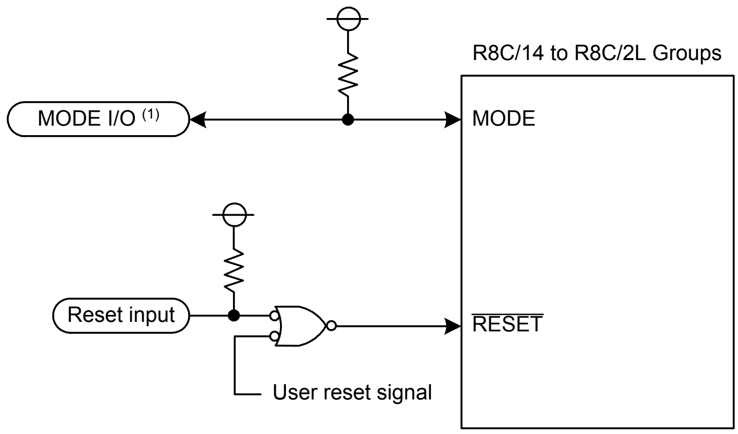
3.4 Assigned Pins

(1) MODE pin
Standard serial I/O mode 2 or standard serial I/O mode 3 is selected according to the MODE pin level after reset is deasserted. This pin also functions as the TXD pin or RXD pin when standard serial I/O mode 3 is selected. When using standard serial I/O mode 3, pull up the MODE pin with approximately 5 kΩ.
(2) Pins TXD1 and RXD1
Pins TXD1 and RXD1 are used as transmit and receive pins in standard serial I/O mode 2. These pins are not used in standard serial I/O mode 3.
(3) RESET pin
A serial programmer controls the RESET pin.
(4) Pins VCC and VSS
When outputting a high or low from a serial programmer, use the voltage according to the MCU's high or low input voltage levels.



Note:
1. Refer to 3.1 Operating Environment.

Figure 3.2 Connection Example in Standard Serial I/O Mode 2



Notes:
1. N-channel open drain output
2. When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit.

Figure 3.3 Connection Example in Standard Serial I/O Mode 3

4. Initial Settings

Perform the following operations sequentially in the boot program initial setting.

(1) Decide a communication format

(2) Adjust bit rates

4.1 Deciding a Communication Format

The communication format is selected from either standard serial I/O mode 2 or standard serial I/O mode 3. 200 ms after reset is deasserted, the MCU enters standard serial I/O mode 2 when the MODE pin level is low, and enters standard serial I/O mode 3 when it is high. Determine the MODE pin level within 100 ms after reset is desserted. The timing diagram is shown in Figure 4.1 Timing to Decide Communication Format. Refer to the hardware user's manual for tw(por1).

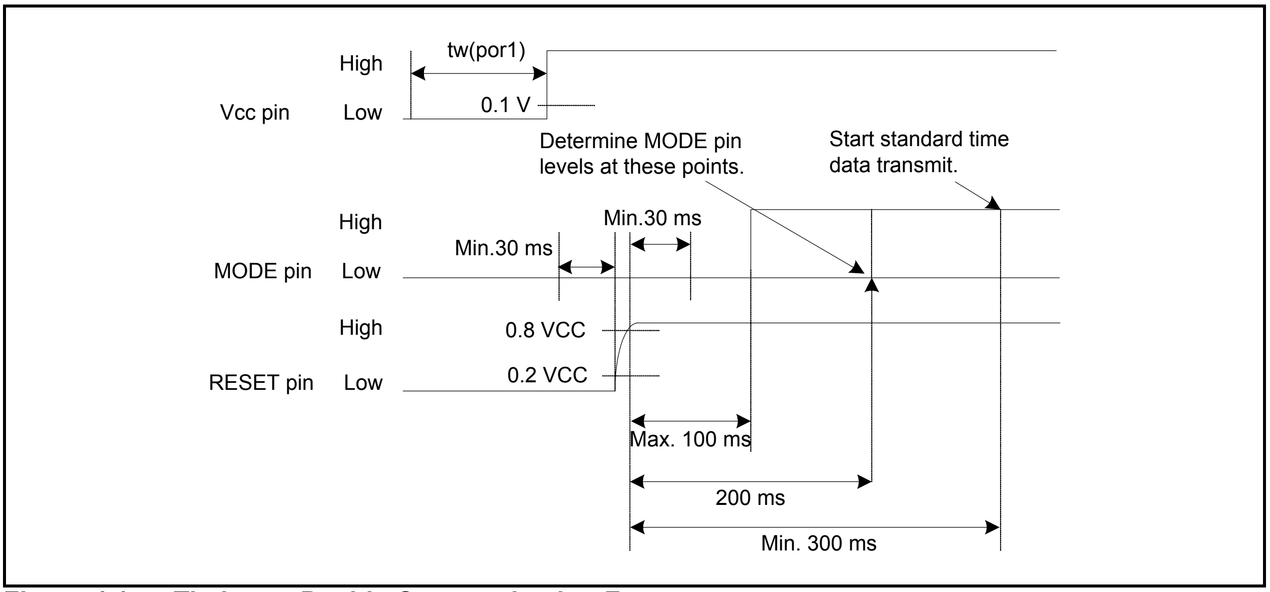


Figure 4.1 Timing to Decide Communication Format

4.2 Adjusting the Bit Rate

The bit rate is adjusted to 9600 bps by receiving the standard time data (00h) 16 times at a bit rate of 9600 bps, and the bit rate 9600 command (B0h) from the serial programmer. When B0h is received successfully, the MCU returns B0h. Figure 4.2 shows the Bit Rate Adjustment Procedure. **Transmit the standard time data at least 300 ms after reset is deasserted.**

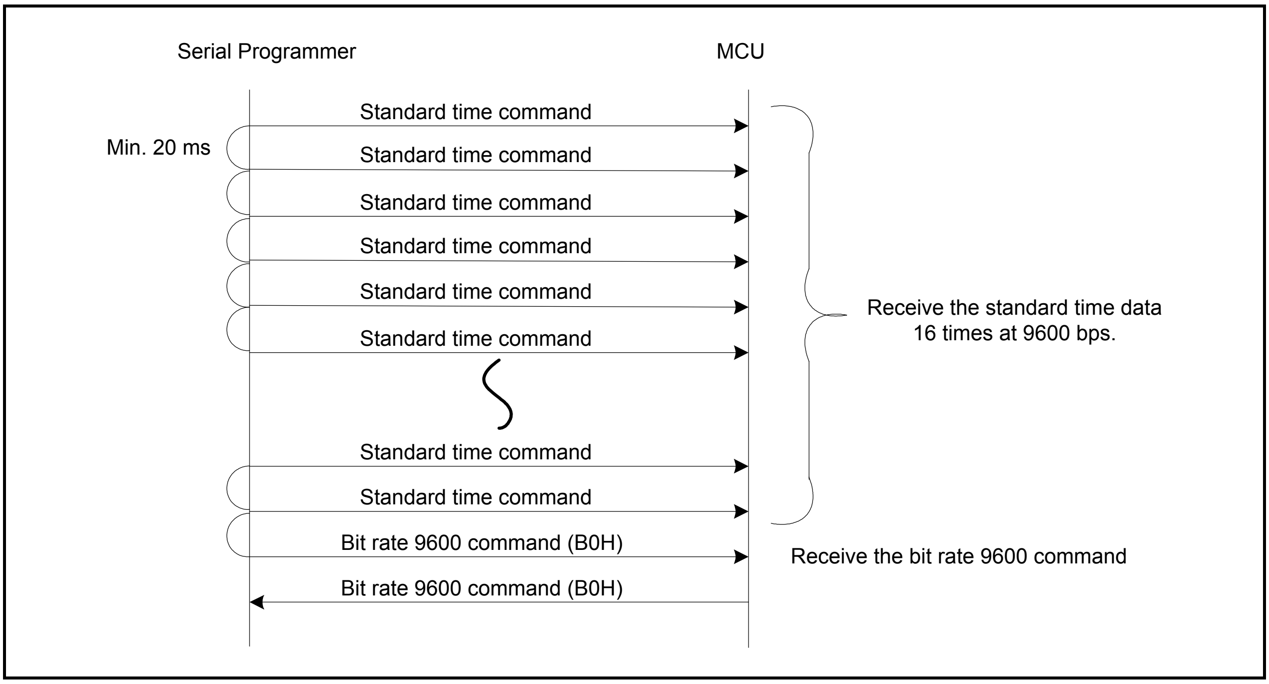


Figure 4.2 Bit Rate Adjustment Procedure

5. Command Specification

5.1 Control Commands

Control commands are listed below

Control Command	1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte	7th Byte or More	ID Not checked
Page read	FFh	Middle-order address	High-order address	Data	Data	Data	Up to data	Acceptance disabled
Page program	41h	Middle-order address	High-order address	Data	Data	Data	Up to data	Acceptance disabled
Unit program	49h	Low-order address	Middle-order address	High-order address	Size	Data	Up to data	Acceptance disabled
Block erase	20h	Middle-order address	High-order address	D0h				Acceptance disabled
Erase all unlocked blocks	A7h	D0h						Acceptance disabled
Read status register	70h	SRD	SRD1					Acceptance enabled
Clear status register	50h							Acceptance disabled
ID data check function	F5h	Low-order address	Middle-order address	High-order address	ID Size	ID1	Up to ID7	Acceptance enabled
Version information output function	FBh	Version	Version	Version	Version	Version	Up to version	Acceptance enabled
Bit rate 9600	B0h	B0h						Acceptance enabled
Bit rate 19200	B1h	B1h						Acceptance enabled
Bit rate 38400	B2h	B2h						Acceptance enabled
Bit rate 57600	B3h	B3h						Acceptance enabled
Bit rate 115200	B4h	B4h						Acceptance enabled
Bit rate setting	B5h	Data	Data					Acceptance enabled
Standard time data	00h							Acceptance enabled

Notes:

1. The shadowed areas show a transfer from the MCU to the serial programmer, the rest shows a transfer from the serial programmer to the MCU.
2. SRD: Status register data; SRD1: Status register data 1
3. All commands can be accepted in blank products.
4. Standard time data is transferred 16 times during initial communication.
5. The number of bytes received is not checked and the timeout error process is not performed in the boot program. Transmit commands with no excess or shortage of data.

6. Commands

6.1 Page Read

6.1.1 Operation

The page read command reads the specified user ROM area in the flash memory in 256-byte units. Specify the area to be read with the high-order address (A16 to A23) and middle-order address (A8 to A15). The target is the 256 bytes from addresses xxxx00h to xxxxFFh.

6.1.2 Packet

	1st Byte	2nd Byte	3rd Byte	4th Byte	Up to 256th Byte
	Command	Address		Data	Up to data
Programmer to MCU	FFh	Middle-order address	High-order address		
MCU to Programmer				Data 0	Up to Data 255

Note:

1. Data 0 is the data to be programmed to low-order address 00h. Data 255 is the data to be programmed to low-order address FFh.

6.1.3 Procedure

(1) Transmit page read command FFh at the first byte.

(2) Transmit the middle-order address at the second byte and the high-order address at the third byte.

(3) Receive the data stored in low-order address 00h sequentially starting from the fourth byte.

6.2 Page Program

6.2.1 Operation

The page program command programs the data to the specified user ROM area in the flash memory in 256-byte units. Specify the area to be programmed with the high-order address (A16 to A23) and middle-order address (A8 to A15). The target is the 256 bytes from addresses xxxx00h to xxxxFFh.

6.2.2 Packet

	1st Byte	2nd Byte	3rd Byte	4th Byte	Up to 256th Byte
	Command	Address		Data	Up to data
Programmer to MCU	41h	Middle-order address	High-order address	Data 0	Up to Data 255
MCU to Programmer					

Note:
1. Data 0 is the data to be programmed to low-order address 00h. Data 255 is the data to be programmed to low-order address FFh.

6.2.3 Procedure

(1) Transmit page program command 41h at the first byte.
(2) Transmit the middle-order address at the second byte and the high-order address at the third byte.
(3) Transmit the programmed data to low-order address 00h sequentially starting from the fourth byte.

When the program data is less than 256 bytes, transmit FFh for the shortage. When the program data is 257 bytes or more, data at the 257th byte is considered to be the data in the next command. If an error occurs during programming, the SR4 bit becomes 1 (program status completed in error).
After executing this command, use the read status register command to confirm the status of the flash memory.

6.3 Unit Program

6.3.1 Operation

The unit program command programs a specified amount of data to the specified user ROM area in the flash memory. Specify the start address of the area to be programmed with the high-order address (A16 to A23), middle-order address (A8 to A15), and low-order address (A0 to A7). Program the specified amount of the program data from the start address.

6.3.2 Packet

	1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte	Up to N Byte
	Command	Address			Number of bytes	Data	Up to data
Programmer to MCU	49h	Low-order address	Middle-order address	High-order address	Size	Data (1)	Data (N)
MCU to Programmer							

Note:

1. Data (1) is the data to be programmed in the start address and Data (N) is the data to be programmed in (start address + N - 1).

6.3.3 Procedure

(1) Transmit unit program command 49h at the first byte.

(2) Transmit the low-order address at the second byte, the middle-order address at the third byte, and the high-order address at the fourth byte.

(3) Transmit the programming size (01h to FFh) at the fifth byte.

(4) Transmit the specified amount of the program data starting from the sixth byte.

If an error occurs during programming, the SR4 bit becomes 1 (program status completed in error).

After executing this command, use the read status register command to confirm the status of the flash memory.

6.4 Block Erase

6.4.1 Operation

The block erase command erases a specified block in the flash memory. Specify a block area with the 8 high-order bits (A16 to A23) and 8 middle-order bits (A8 to A15) at the given address of the block to be erased.

6.4.2 Packet

	1st Byte	2nd Byte	3rd Byte	4th Byte	Up to 256th Byte
	Command	Block Address			
Programmer to MCU	20h	Middle-order address	High-order address	D0h	
MCU to Programmer					

6.4.3 Procedure

(1) Transmit block erase command 20h at the first byte.
(2) Transmit the middle-order address at the second byte and the high-order address at the third byte.
(3) Transmit confirmation command D0h at the fourth byte.

After receiving confirmation command D0h, erasing on the specified block starts. Erasing sets all data in the specified block to FFh. If an error occurs during erasing, the SR5 bit becomes 1 (erase status completed in error). **After executing this command, use the read status register command to confirm the status of the flash memory.**

6.5 Erase All Unlocked Blocks

6.5.1 Operation

The erase all unlocked blocks command erases the entire user ROM area (data flash area and program area) in the flash memory.

6.5.2 Packet

	1st Byte	2nd Byte	3rd Byte	4th Byte	Up to 256th Byte
	Command				
Programmer to MCU	A7h	D0h			
MCU to Programmer					

6.5.3 Procedure

(1) Transmit erase all unlocked block command A7h at the first byte.
(2) Transmit confirmation command D0h at the second byte.

After receiving confirmation command D0h, erasing on all blocks starts. Erasing sets all data in the flash memory to FFh. If an error occurs during erasing, the SR5 bit becomes 1 (erase status completed in error).
After executing this command, use the read status register command to confirm the status of the flash memory.

6.6 Read Status Register

6.6.1 Operation

The read status register command confirms the operating status of the flash memory.

6.6.2 Packet

	1st Byte	2nd Byte	3rd Byte	4th Byte	Up to 256th Byte
	Command	SRD			
Programmer to MCU	70h				
MCU to Programmer		SRD output	SRD1 output		

6.6.3 Procedure

(1) Transmit read status register command 70h at the first byte.
(2) Receive SRD at the second byte.
(3) Receive SRD1 at the third byte.

6.6.4 SRD Register

Bit in SRD	Status Name	Definition	
		1	0
SR7 (bit 7)	Sequencer status	Ready	Busy
SR6 (bit 6)	Reserved		
SR5 (bit 5)	Erase status	Completed in error	Completed normally
SR4 (bit 4)	Program status	Completed in error	Completed normally
SR3 (bit 3)	Reserved		
SR2 (bit 2)	Reserved		
SR1 (bit 1)	Reserved		
SR0 (bit 0)	Reserved		

(1) Sequencer status
The sequencer status shows the operating status of the flash memory. This bit becomes 0 (busy) during auto-programming or auto-erasure. This bit becomes 1 (ready) when auto-programming or auto-erasure is completed.

(2) Erase status
The erase status shows the erase operating status. If an error occurs, this bit becomes 1. This bit becomes 0 when the clear status register command is executed.

(3) Program status
The program status shows the programming status. If an error occurs, this bit becomes 1. This bit becomes 0 when the clear status register command is executed.

Bits SR5 and SR4 become 1 under the following:
• When a defined command is not input successfully.
• When data other than D0h or FFh is input in the input cycle for the block erase confirmation command. If FFh is input, the command is cancelled and the MCU enters read array mode.

(4) Reserved bit
The read value is undefined.

6.6.5 SRD1 Register

Bit in SRD1	Status Name	Definition	
		1	0
SR15 (bit 7)	Reserved		
SR14 (bit 6)	Reserved		
SR13 (bit 5)	Reserved		
SR12 (bit 4)	Reserved		
SR11 (bit 3)	ID checked bits	00: Not checked 01: Not matched 10: Reserved 11: Checked	
SR10 (bit 2)			
SR9 (bit 1)	Reserved		
SR8 (bit 0)	Reserved		

(1) ID checked bits
These bits show the ID checked result.

(2) Reserved
The read value is undefined.

6.7 Clear Status Register

6.7.1 Operation

The clear status register command initializes the status register. Use this command to initialize the status register before erasing the flash memory and performing the page program.

6.7.2 Packet

	1st Byte	2nd Byte	3rd Byte	4th Byte	Up to 256th Byte
	Command				
Programmer to MCU	50h				
MCU to Programmer					

6.7.3 Procedure

(1) Transmit clear status register command 50h at the first byte.

After executing this command, use the read status register command to confirm the status of the flash memory.

6.8 ID Data Check Function

6.8.1 Operation

The ID data check function command checks if the 7-byte ID stored in the flash memory matches the 7-byte ID transmitted from the serial programmer. Some commands are not accepted if these IDs mismatch in the ID check function.

6.8.2 Packet

	1st Byte	2nd Byte	3rd Byte	4th Byte	5th Byte	6th Byte	Up to 12th Byte
	Command	Address			ID size	ID	ID
Programmer to MCU	F5h	DFh	FFh	00h	07h	ID1	Up to ID7
MCU to Programmer							

Note:
1. DFh, FFh, and 00h are the addresses in which ID1 is stored.

6.8.3 Procedure

(1) Transmit ID data check function command F5h at the first byte.
(2) Transmit the low-order address where ID1 is stored at the second byte, the middle-order address at the third byte, and the high-order address at the fourth byte.
(3) Transmit the number of IDs (07h) at the fifth byte.
(4) Transmit IDs from the sixth byte to the 12th byte.

After transmission, the ID checked result is reflected in bits SR10 and SR11. If the transmitted address is not the ID address, or if the ID size is not 7, the ID check function recognizes a data mismatch even if those IDs match. **After executing this command, use the read status register command to confirm the status of the flash memory.**

6.9 Version Information Output Function

6.9.1 Operation

The version information output function command is used to confirm the boot program version.

6.9.2 Packet

	1st Byte	2nd Byte	3rd Byte	4th Byte	Up to 9th Byte
	Command				
Programmer to MCU	FBh				
MCU to Programmer		V	E	R	X

Note:

1. Version information is received from V as VER. X.XX (X: numbers) as eight of ASCII characters.

6.9.3 Procedure

(1) Transmit version information output function command FBh at the first byte.

(2) Receive the version information from the second byte to the ninth byte as ASCII characters.

6.10 Bit Rate 9600

6.10.1 Operation

The bit rate 9600 command changes the bit rate to typ. 9600 bps. When an external oscillator is necessary in standard serial I/O mode 2, a bit rate error due to frequency error may occur. Change the bit rate to typ. 9615 bps in standard serial I/O mode 3.

6.10.2 Packet

	1st Byte	2nd Byte
	Command	
Programmer to MCU	B0h	
MCU to Programmer		B0h

6.10.3 Procedure

(1) Transmit bit rate 9600 command B0h at the first byte.
(2) Receive confirmation command B0h at the second byte.
(3) Set the bit rate to typ. 9600 bps in the boot program after transmitting the confirmation command.

6.11 Bit Rate 19200

6.11.1 Operation

The bit rate 19200 command changes the bit rate to typ. 19200 bps. When an external oscillator is necessary in standard serial I/O mode 2, a bit rate error due to frequency error may occur. Change the bit rate to typ. 19230 bps in standard serial I/O mode 3.

6.11.2 Packet

	1st Byte	2nd Byte
	Command	
Programmer to MCU	B1h	
MCU to Programmer		B1h

6.11.3 Procedure

(1) Transmit bit rate 19200 command B1h at the first byte.
(2) Receive confirmation command B1h at the second byte.
(3) Set the bit rate to typ. 19200 bps in the boot program after transmitting the confirmation command.

6.12 Bit Rate 38400

6.12.1 Operation

The bit rate 38400 command changes the bit rate to typ. 38400 bps. When an external oscillator is necessary in standard serial I/O mode 2, a bit rate error due to frequency error may occur. Change the bit rate to typ. 38461 bps in standard serial I/O mode 3.

6.12.2 Packet

	1st Byte	2nd Byte
	Command	
Programmer to MCU	B2h	
MCU to Programmer		B2h

6.12.3 Procedure

(1) Transmit bit rate 38400 command B2h at the first byte.
(2) Receive confirmation command B2h at the second byte.
(3) Set the bit rate to typ. 38400 bps in the boot program after transmitting the confirmation command.

6.13 Bit Rate 57600

6.13.1 Operation

The bit rate 57600 command changes the bit rate to typ. 57600 bps. When an external oscillator is necessary in standard serial I/O mode 2, a bit rate error due to frequency error may occur. Change the bit rate to typ. 55555 bps in standard serial I/O mode 3.

6.13.2 Packet

	1st Byte	2nd Byte
	Command	
Programmer to MCU	B3h	
MCU to Programmer		B3h

6.13.3 Procedure

(1) Transmit bit rate 57600 command B3h at the first byte.
(2) Receive confirmation command B3h at the second byte.
(3) Set the bit rate to typ. 57600 bps in the boot program after transmitting the confirmation command.

6.14 Bit Rate 115200

6.14.1 Operation

The bit rate 115200 command changes the bit rate to typ. 115200 bps. When an external oscillator is necessary in standard serial I/O mode 2, a bit rate error due to frequency error may occur. **This command does not apply in standard serial I/O mode 3.**

6.14.2 Packet

	1st Byte	2nd Byte
	Command	
Programmer to MCU	B4h	
MCU to Programmer		B4h

6.14.3 Procedure

(1) Transmit bit rate 115200 command B4h at the first byte.
(2) Receive confirmation command B4h at the second byte.
(3) Set the bit rate to typ. 115200 bps in the boot program after transmitting the confirmation command.

6.15 Bit Rate Setting

6.15.1 Operation

The bit rate setting command transmits the data set to the bit rate register in the boot program.

6.15.2 Packet

	1st Byte	2nd Byte	3rd Byte
	Command	Setting value	
Programmer to MCU	B5h	Data	
MCU to Programmer			Data

6.15.3 Procedure

(1) Transmit bit rate setting command B5h at the first byte.
(2) Transmit the data set to the bit rate register at the second byte.
(3) Receive the confirmation command (data transmitted at the second byte) at the third byte.
(4) Set the received data to the bit rate register in the boot program after transmitting the confirmation command.

6.15.4 Communication Bit Rate

The high-speed on-chip oscillator (typ. 8 MHz) is used for the BRG count source in the boot program in standard serial I/O mode 3. Bit rates set in the boot program in standard serial I/O mode 3 are shown below.

Data (BRG setting value)	Bit Rate (bps)
33h	9615
19h	19230
0Ch	38461
08h	55555
03h	125000
01h	250000
00h	500000

7. Timing

7.1 Data Transmit Interval (Between Bytes)

Transmit the standard time data for a minimum of 20 ms and control command for a minimum of 5 µs. This transmit interval is required in the boot program as the receive process time. This process time is for reference when the CPU clock is typ. 8 MHz. Adjust values according to the oscillation frequency shown below when the CPU clock is selected as external oscillator frequency no division.

	2 MHz	8 MHz	16 MHz
Standard time data	Min. 80 ms	Min. 20 ms	Min. 10 ms
Control command	Min. 20 µs	Min. 5 µs	Min. 2.5 µs

7.2 Switching from Transmission to Reception in Standard Serial I/O Mode 3

Switch from reception to transmission after 2 ms elapses, and from transmission to reception within 500 µs.

7.3 Read Status Register Command

The boot program transmits the content in the SRD register after programming or erasure by transmitting the read status register command after transmitting the page program, unit program, block erase, and erase all unlocked blocks commands. Refer to the Electrical Characteristics chapter in the hardware user's manual for program and erase times.

8. Note

8.1 Read status register

Even if an error occurs during writing, the SR4 bit may not become 1 (program status is terminated by error). After writing, always read data and confirm that expected value is written.

9. Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

Revision History	R8C/1x, 2x Series R8C/1x, 2x Series Standard Serial I/O Mode Protocol Specification

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 1, 2010	—	First edition issued
1.01	Oct. 13, 2011	24	An error in 8.1 Read status register revised

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141