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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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H8S Family

Using the User Branch Function to Clear External WDT during Flash Memory Programming/Erasing

Introduction

The user branch function enables the execution of a user processing routine once every processing unit of a predetermined size during flash-memory programming or erasing.

The flash-memory programming/erasing processing consists of several steps, including the application of programming pulses and reading for verification. The user branch function can be used to execute a user processing routine in the intervals between these steps.

The sample task of this application note shows how to use the user branch function to clear an external watchdog timer (external WDT) and thus avoid an MCU reset during the erasure of flash memory.

Target Device

H8S/2378R

Preface

Other than the target device indicated above, the program covered in this application note can be run on H8S devices that have the same I/O registers as those employed by the program. However, since some functional modules may be changed for the addition of functionality etc., be sure to perform a thorough evaluation by confirming the details with the hardware manual for the actual target device.

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1. Specifications

This sample task shows how to apply the user branch function to clear an external WDT during flash-memory erasure. Specifications of this sample task are given below. An example of the connection for this sample task is shown in figure 1.

- (1) The external WDT is a reset IC with on-chip watchdog timer (M62050) manufactured by Renesas Technology for 3-V power-supply systems. The only functionality of the M62050 watchdog timer used in this sample task is the watchdog timer. The period of the watchdog timer is set to 120 ms. For details, see the M62050 datasheet.
- (2) The external WDT outputs a reset signal when it does not have an incoming clearing signal within 120 ms. As long as the external WDT continues to receive consecutive clearing signals on the external WDT input (WD) pin, the M62050 maintains the $\overline{\text{RST1}}$ pin at the high level. When input of the clearing signal for the external WDT stops, a low-level signal (reset signal) is output on the $\overline{\text{RST1}}$ pin to reset the H8S MCU.
- (3) Only one block of EB9 (64-KB area) in the flash memory is selected for erasure. Erasing EB9 (a 64-KB area) takes up to 750 ms. Consequently, when the setting time for the external WDT is 120 ms, a conventional MCU will be reset by the external WDT during processing to erase the flash memory because the interval for clearing the external WDT is greater than the period set for the WDT.
- (4) In this sample task, this is prevented by employing the user branch function to issue external WDT clearing signals on the P10 pin before the interval set for the external WDT elapses. The H8S MCU thus clears the external WDT and continues processing for flash-memory erasure.

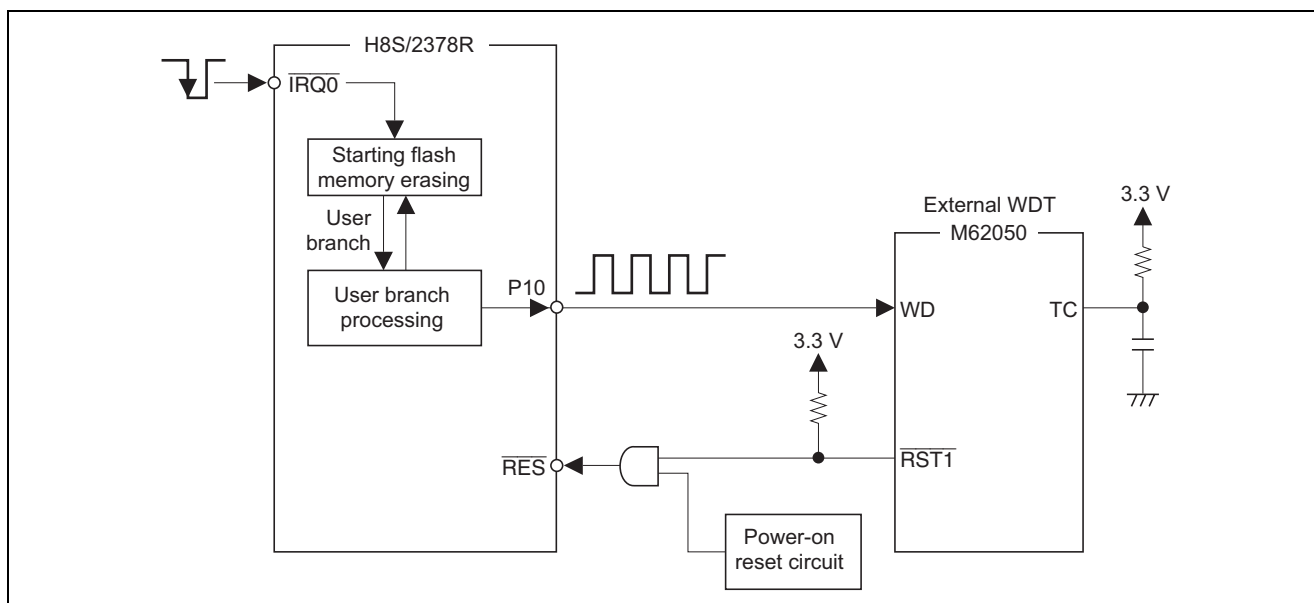


Figure 1 External WDT Connection Diagram

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Setting
Operating frequency	Input clock : 8.25 MHz
	System clock : 33 MHz (input clock frequency × 4)
Operating mode	Mode 7 (single chip mode)
	Mode pin settings: MD2 = 1, MD1 = 1, MD0 = 1
Onboard programming mode	User program mode

3. Description of Modules Used

3.1 User Branch Function

The programming processing is performed in 128-byte units. It consists the program pulse application, verify read, and several other steps. Erasing is performed in one divided-block units and consists of several processing steps. The user processing routine can be executed between the steps, this setting for which is called the user branch addition.

3.2 Setting FPEFEQ and FUBRA Parameters

To employ the user branch function, the FPEFEQ and FUBRA parameters must be set from the processing to initialize the flash-memory programming and erasing programs.

- The frequency setting bits (F15 to F0) of the FPEFEQ parameter (general register: ER0) are set to the value that corresponds to the current frequency of the CPU clock.
The allowable setting range for the FPEFEQ parameter is 8 MHz to 34 MHz*. When the setting is for a frequency beyond this range, an error code is returned in the FPFR parameter of the initialization program and initialization does not proceed.
- The first address of the user branch destination is set in the FUBRA parameter (general register: ER1) and the user branch enable bits (FUBE15 to 0) are set in the FPEFEQ parameter (general register: ER0). To enable the user branch function, set FUBE15–0 = H'AA55. To disable the user branch function, set FUBRA and FUBE15–0 to 0.
When the user branch function is made, the user branch destination code must be executed from a space other than the user MAT to be programmed. Furthermore, the destination cannot be set within the area for the downloaded on-chip programs. Execute a RTS instruction to return from user-branch processing to programming processing.

Note: * 8 to 35 MHz for the H8S/2378.

Detailed descriptions of the FPEFEQ and FUBRA parameters are given in (a) and (b).

(a) Flash programming/erasing frequency parameter (FPEFEQ: general register ER0 of CPU)

This parameter sets the operating frequency of the CPU and enables the user branch function.

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	FUBE15 to 0	—	R/W	Flash User Branch Enable Bits Set these bits to H'AA55 to enable the user branch function. Otherwise, set to H'0000.
15 to 0	F15 to F0	—	R/W	Frequency Set Set the operating frequency of the CPU. The setting value must be calculated as the following methods. <ul style="list-style-type: none"> The operating frequency which is shown in MHz units must be rounded in a number to three decimal places and be shown in a number of two decimal places. The value multiplied by 100 is converted to the binary digit and is written to the FPEFEQ parameter (general register ER0). For example, when the operating frequency of the CPU is 35.000 MHz, the value is thus as follows. <ul style="list-style-type: none"> The number to three decimal places of 35.000 is rounded and the value is thus 35.00. The formula that $35.00 \times 100 = 3500$ is converted to the binary digit and B'0000,1101,1010,1100 (H'0DAC) is set to R0.

(b) Flash user branch address set parameter (FUBRA: general register ER1 of CPU)

This parameter sets the user branch destination address. A specified user routine can be used to perform programming or erasing of processing units of predetermined size. When using the user branch function, set the flash user branch enable bits in FPEFEQ to H'AA55.

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	UA31 to UA0	—	R/W	<p>Flash User Branch Enable</p> <p>User branch destination address</p> <p>The user branch destination should be located in a space in RAM other than that to which on-chip programs are transferred or the external bus space.</p> <p>Be careful not to cause program runaway by branching to an area without execution codes, and do not destroy an area to which on-chip programs are downloaded or a stack area. The contents of flash memory cannot be guaranteed if program runaway occurs or if download or stack areas are destroyed.</p> <p>The user branch destination processing should not initiate downloading of on-chip programs, initialization, programming, or erasing. Programming or erasing cannot be guaranteed when returning from the user branch destination. Also, take care not to rewrite previously prepared programming data.</p> <p>Furthermore, do not rewrite program/erase interface registers as part of the user branch destination processing.</p> <p>After user branch processing completes, use the RTS instruction to return to the program/erase program.</p>

3.3 User Branch Processing Intervals

The user branch processing interval differs for programming and erasing operations. Table 2 shows the maximum start intervals when the CPU clock frequency is 35 MHz.

Table 2 Use Branch Processing Start Intervals

	Maximum interval
Programming operation	1 ms
Erasing operation	30 ms

4. Principles of Operation

This sample task shows how to use the user branch function so that the WDT clearing signal is output during flash-memory erasure.

Figure 2 shows the operation of this sample task. Figure 3 shows the timing of operations in this sample task. Details of figures 2 and figure 3 are given below. Points labeled (1) to (4) in figures 2 and 3 correspond to descriptions (1) to (4) below.

- (1) In this sample task, a power-on reset is applied in user mode. Input of a falling edge to the $\overline{\text{IRQ0}}$ pin causes a transition to user program mode and then initiates erasure processing.
- (2) During initialization processing for flash-memory erasure, parameters FPEFEQ and FUBRA are set to enable the user branch function. These settings allow the execution of user branch processing between the steps for erasing flash memory.
- (3) The initiation interval for user branch processing during erasure processing is up to 30 ms. Since the user branch processing inverts the output on the P10 pin, a high-level signal (external WDT clearing signal) is output on the P10 pin and clears the external WDT at least once every 60 ms ($30 \text{ ms} \times 2$). This clearing interval is less than the external WDT setting time (120 ms), allowing continued operation without resetting of flash-memory erasure processing by the WDT.
- (4) When the erasure of flash memory is complete, a transition is made to user mode. At this point, the external WDT is cleared by normal user processing.

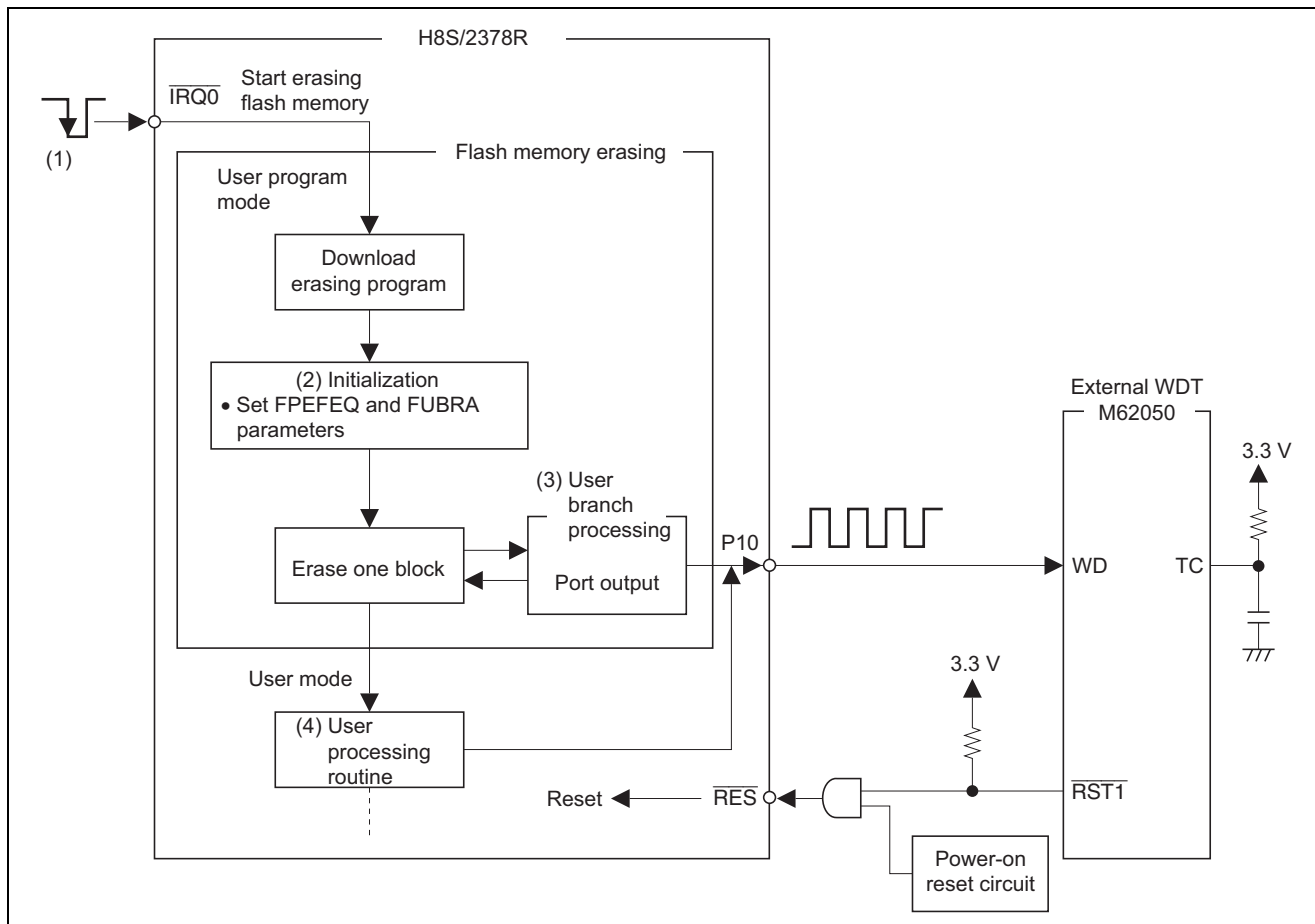


Figure 2 Details of Operation

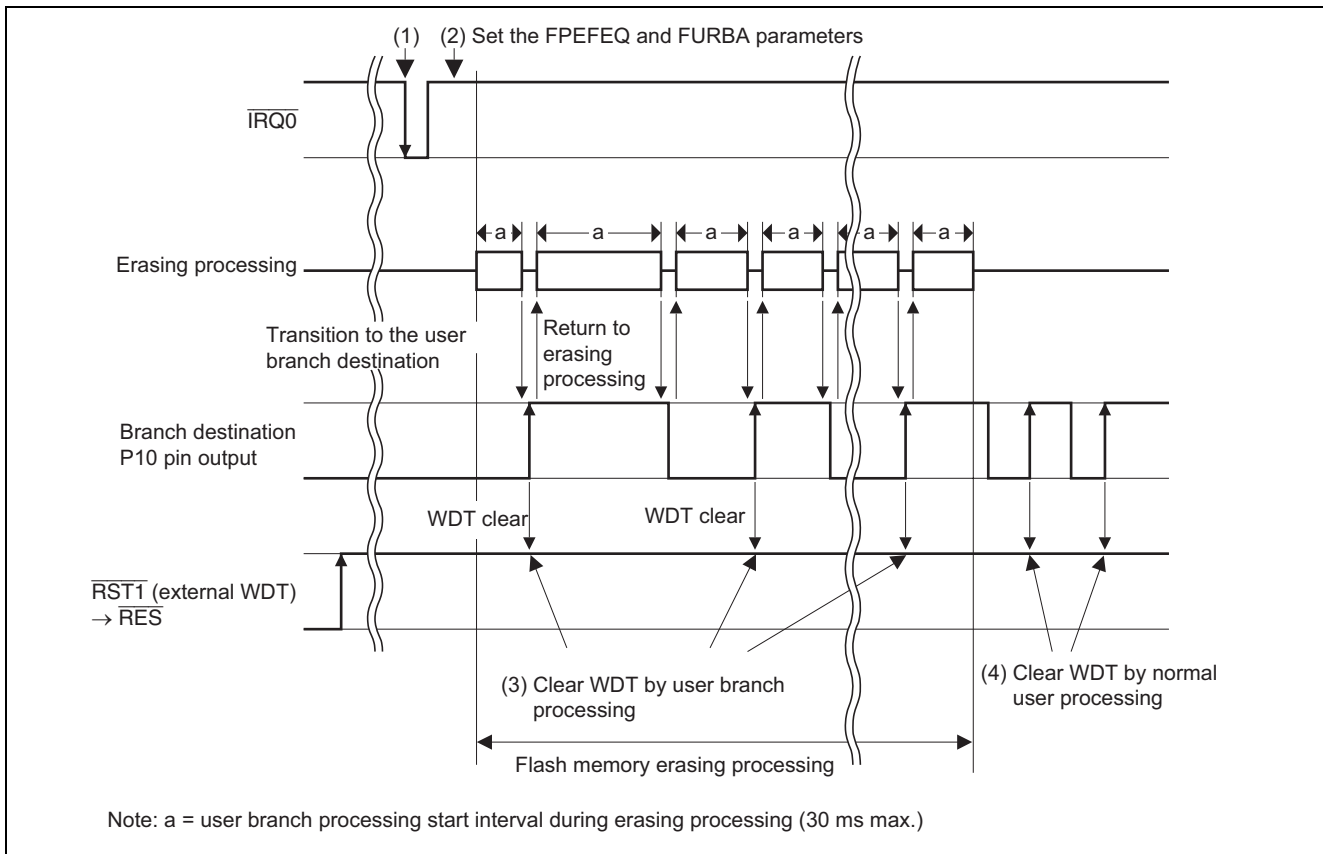


Figure 3 Operation Timing

5. Description of Software

5.1 Operating Environment

Table 3 Operating Environment

Item	Details
Development tool	High-performance Embedded Workshop Ver.4.03.00
C/C++ compiler	H8S,H8/300 SERIES C/C++ Compiler Ver6.02.00 (manufactured by Renesas Technology) Option settings: -cpu = 2000A:24, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register,shift,struct,expression)
Optimizing linkage editor	Optimizing Linkage Editor Ver.9.03.00 (manufactured by Renesas Technology) Option settings: -rom = PFL_Code = RAM

Table 4 Section Settings

Address	Section Name	Description
H'001000	P	Program area
	PFL_Code	Area where the erasing-procedure program is stored
H'010000	CSMPL	Target area for erasure = erase block 9 (EB9)
H'FF4000	RAM	Area for transfer of the erasing-procedure program

Table 5 Vector Table for Interrupt Exception Handling

Exception Handling Source	Vector No.	Address in Vector Table	Destination Interrupt-Processing Function
Reset	0	H'000000	init

5.2 List of Functions

A list of functions for the main program is given in table 6. A list of functions for the flash-memory erasure procedure program is given in table 7. The hierarchy of calls in the user program is shown in figure 4.

Table 6 List of Functions for Main Program

Function Name	Function
init	Initialization routine Releases the modules from module stop mode, configures the clocks, and calls the main function.
main	Main routine Transfers the flash-memory erasing-procedure program to the on-chip RAM and calls the flew_main function.
copyfzram	Transfers the flash-memory erasure procedure program to the on-chip RAM.

Table 7 List of Functions for Flash-Memory Erasure Procedure Program

Function Name	Function
flew_main	Main routine of the flash-memory erasure procedure program
download	Download of on-chip erasing program
fw_init	Flash-memory erasure initialization Sets the FPEFEQ and FUBRA parameters.
erase_process	Flash-memory erasure
UB_WDTclear	User branch processing User processing routine at the user branch destination. This produces clearing signals for the external WDT on the P10 pin.

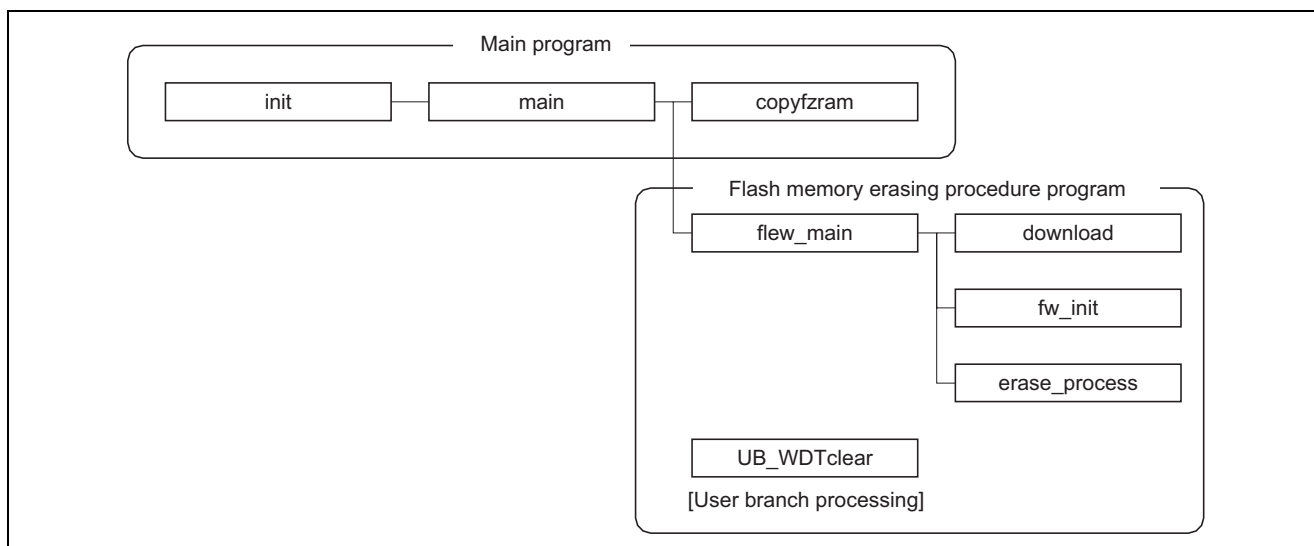


Figure 4 Hierarchical Structure

5.3 Description of Constants

A list of constants for the flash-memory erasure procedure program is given Table 8 and table 9.

Table 8 List of Symbolic Constants

Constant Name	Setting	Description	Used In
WKAREA	0	Specifies the destination address for downloading of an on-chip program. 0: Sets the address where downloading starts to H'FF9000. 1: Sets the address where downloading starts to H'FFA000. 2: Sets the address where downloading starts to H'FFB000. 3: Sets the address where downloading starts to H'FF8000.	download
CLOCK	3300	System Clock Set $33.00 \times 100 = 3300$ when the system clock is 33.00 MHz.	fw_init
DWNLDTOP	0x00FF8000	Start address to download the on-chip program	—
FLSHWK	(WKAREA==3?DWNLDTOP:(DWNLDTOP+((1+WKAREA)*0x1000)))	Used to calculate the address where downloading of an on-chip program starts	—
DPFR	*(volatile unsigned char *)FLSHWK	Start address to store the return value of the on-chip program download result	download
ERASE_ENT	(FLSHWK+0x10)	Start address of the erasing program	erase_process
INIT_ENT	(FLSHWK+0x20)	Start address of the initialization program	fw_init

Table 9 List of const Constants

Type	Variable/Array Name	Setting	Description	Used In
unsigned char	SAMPLEDT [0x10000]	H'00 ... H'00	Array used to write 0 to all locations in EB9 (64-KB area). This is a dummy array that is only used to test the operation of the erasing program and is not used in actual operations.	—

5.4 Description of Functions for Main Program

5.4.1 init Function

1. Functional overview

Initialization routine: releases the modules from module stop mode, configures the clocks, and calls the main function.

2. Arguments

None

3. Return value

None

4. Description of internal registers used

The internal registers used in this sample task are listed below. Note that the settings shown below are for this sample task and are not initial values.

- System clock control register (SCKCR) Number of bits: 8 Address: H'FFFF3B

Bit	Bit Name	Setting	R/W	Function
2	SCK2	0	R/W	System Clock Select 2 to 0
1	SCK1	0	R/W	Select the division ratio.
0	SCK0	0	R/W	000: 1/1

- Mode control register (MDCR) Number of bits: 8 Address: H'FFFF3E

Bit	Bit Name	Setting	R/W	Function
2	MDS2	—*	R	Mode Select 2 to 0
1	MDS1	—*	R	These bits indicate the input levels at pins MD2 to MD0 (the current operating mode). Bits MD2 to MD0 correspond to MD2 to MD0. MDS2 to MDS0 are read-only bits and they cannot be modified. The mode pin (MD2 to MD0) input levels are latched into these bits when MDCR is read. These latches are released by a reset.
0	MDS0	—*	R	

Note: * Determined by the settings on pins MD2 to MD0.

- MSTPCRH and MSTPCRL control module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop mode, while clearing the bit to 0 release the module from module stop mode.

- Module stop control register H (MSTPCRH) Number of bits: 8 Address: H'FFFF40

Bit	Bit Name	Setting	R/W	Target Module
15	ACSE	0	R/W	All-Module-Clocks-Stop Mode Enable Enables or disables all-module-clocks-stop mode, in which, when the CPU executes a SLEEP instruction after module stop mode has been set for all the on-chip peripheral functions controlled by MSTPCR or the on-chip peripheral functions except the TMR. 0: All-module-clocks-stop mode disabled 1: All-module-clocks-stop mode enabled
14	MSTP14	1	R/W	EXDMA controller (EXDMAC)
13	MSTP13	1	R/W	DMA controller (DMAC)
12	MSTP12	1	R/W	Data transfer controller (DTC)
11	MSTP11	1	R/W	16-bit timer-pulse unit (TPU)
10	MSTP10	1	R/W	Programmable pulse generator (PPG)
9	MSTP9	1	R/W	D/A converter (channels 0 and 1)
8	MSTP8	1	R/W	D/A converter (channels 2 and 3)

- Module stop control register L (MSTPCRL) Number of bits: 8 Address: H'FFFF41

Bit	Bit Name	Setting	R/W	Target Module
7	MSTP7	1	R/W	D/A converter (channels 4 and 5)
6	MSTP6	1	R/W	A/D converter
5	MSTP5	1	R/W	Serial communicationsinterface_4 (SCI_4)
4	MSTP4	1	R/W	Serial communicationsinterface_3 (SCI_3)
3	MSTP3	1	R/W	Serial communicationsinterface_2 (SCI_2)
2	MSTP2	1	R/W	Serial communicationsinterface_1 (SCI_1)
1	MSTP1	1	R/W	Serial communicationsinterface_0 (SCI_0)
0	MSTP0	1	R/W	8-bit timer (TMR)

- EXMSTPCR performs all-module-clocks-stop mode control with MSTPCR. When entering all-module-clocks-stop mode, set EXMSTPCR to H'FFFF. Otherwise, set EXMSTPCR to H'FFFD.

- Extension module stop control register H (EXMSTPCRH) Number of bits: 8 Address: H'FFFF42

Bit	Bit Name	Setting	R/W	Target Module
15 to 12	—	0	R/W	Reserved Read/write is enabled. 1 should be written in writing.

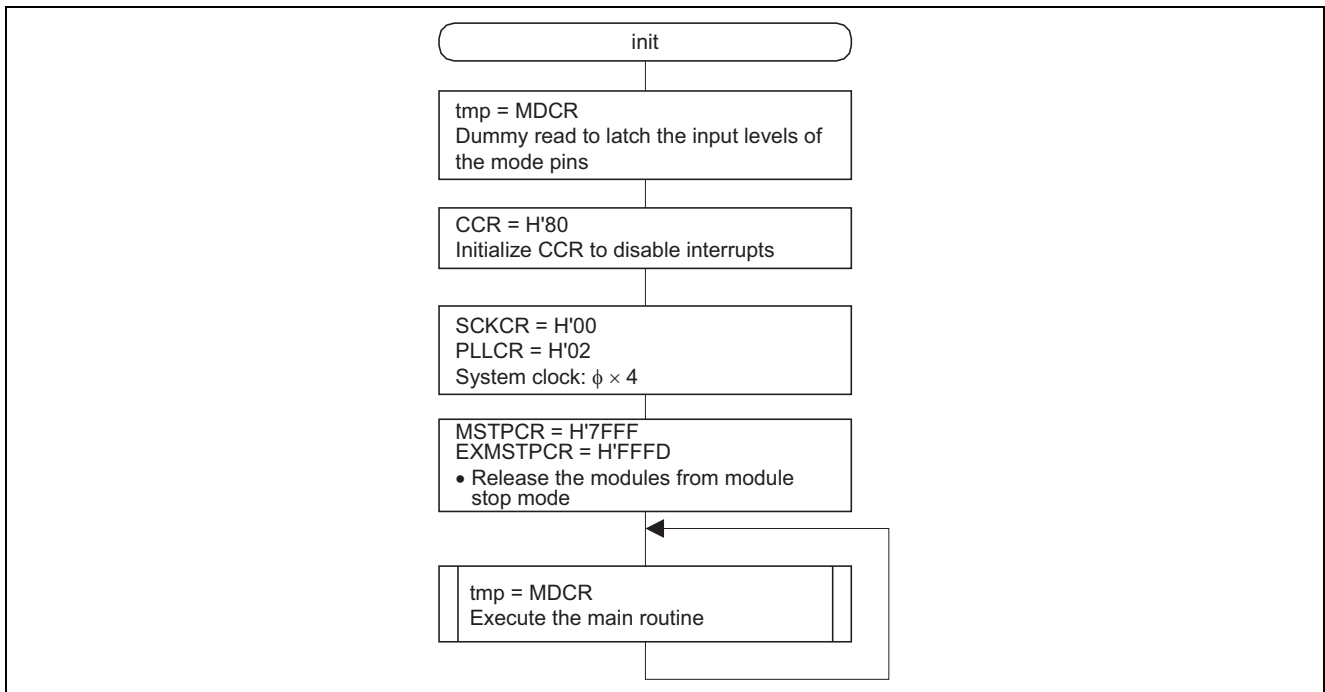
- Extension module stop control register L (EXMSTPCR) Number of bits: 8 Address: H'FFFF43

Bit	Bit Name	Setting	R/W	Target Module
4	MSTP20	1	R/W	I ² C bus interface 2_1 (IIC2_1)
3	MSTP19	1	R/W	I ² C bus interface 2_0 (IIC2_0)

- PLL control register (PLLCR) Number of bits: 8 Address: H'FFFF45

Bit	Bit Name	Setting	R/W	Function
1	STC1	1	R/W	Frequency Multiplication Factor
0	STC0	0	R/W	These bits specify the frequency multiplication factor used by the PLL circuit. 10: ×4

5. Flowchart



5.4.2 main Function

1. Functional overview

Main routine: transfers the flash-memory erasure procedure program to the on-chip RAM and calls the `flew_main` function.

2. Arguments

None

3. Return value

None

4. Description of internal registers used

The internal registers used in this sample task are listed below. Note that the settings shown below are for this sample task and are not initial values.

- IRQ pin select register (ITSR) Number of bits: 16 Address: H'FFFE16

Bit	Bit Name	Setting	R/W	Function
0	ITS0	0	R/W	Selects $\overline{\text{IRQ0}}$ input pin. 0: P50 1: P80

- IRQ sense control register L (ISCRL) Number of bits: 16 Address: H'FFFE1C

Bit	Bit Name	Setting	R/W	Function
1	IRQ0SCB	0	R/W	IRQ0 Sense Control B
0	IRQ0SCA	1	R/W	IRQ0 Sense Control A 01: Interrupt request generated at falling edge of $\overline{\text{IRQ0}}$.

- Port 1 data direction register (P1DDR) Number of bits: 8 Address: H'FFFE20

Bit	Bit Name	Setting	R/W	Function
0	P10DDR	1	R/W	0: Sets the P10 pin as input. 1: Sets the P10 pin as output.

- Port D data direction register (PDDDR) Number of bits: 8 Address: H'FFFE2C

Bit	Bit Name	Setting	R/W	Function
7	PD7DDR	1	R/W	0: Sets the PD7 pin as input. 1: Sets the PD7 pin as output.

• IRQ status register (ISR) Number of bits: 16 Address: H'FFFF34

Bit	Bit Name	Setting	R/W	Function
0	IRQ0F	—	R/(W)*	[Setting condition] Occurrence of the interrupt sources selected by ISCR [Clearing condition] <ul style="list-style-type: none"> • Writing of 0 after having read as 1 • Execution of interrupt exception handling when low-level detection is set and IRQ0 input is high • Execution of IRQ0 interrupt exception handling when falling, rising, or both-edge detection is set • The DTC activation by an IRQ0 interrupt, and clearing of the DISEL bit in MRB of the DTC to 0

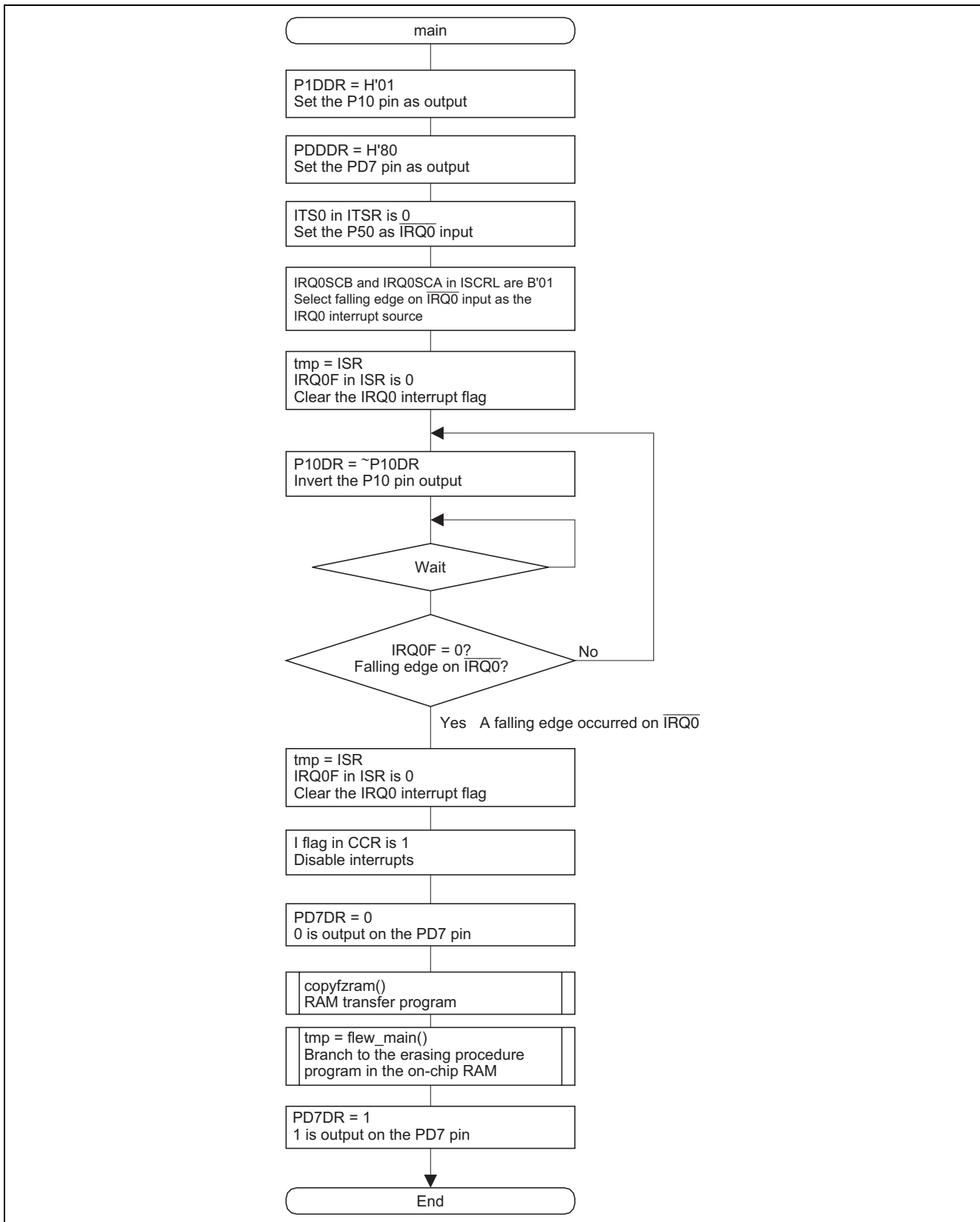
• Port 1 data register (P1DR) Number of bits: 8 Address: H'FFFF60

Bit	Bit Name	Setting	R/W	Function
0	P10DR	0/1	R/W	0: The P10 pin is low. 1: The P10 pin is high.

• Port D data register (PDDR) Number of bits: 8 Address: H'FFFF6C

Bit	Bit Name	Setting	R/W	Function
7	PD7DR	0/1	R/W	0: The PD7 pin is low. 1: The PD7 pin is high.

5. Flowchart



5.4.3 copyfzram Function

1. Functional overview

This function transfers the flash-memory erasure procedure program to the on-chip RAM.

2. Arguments

None

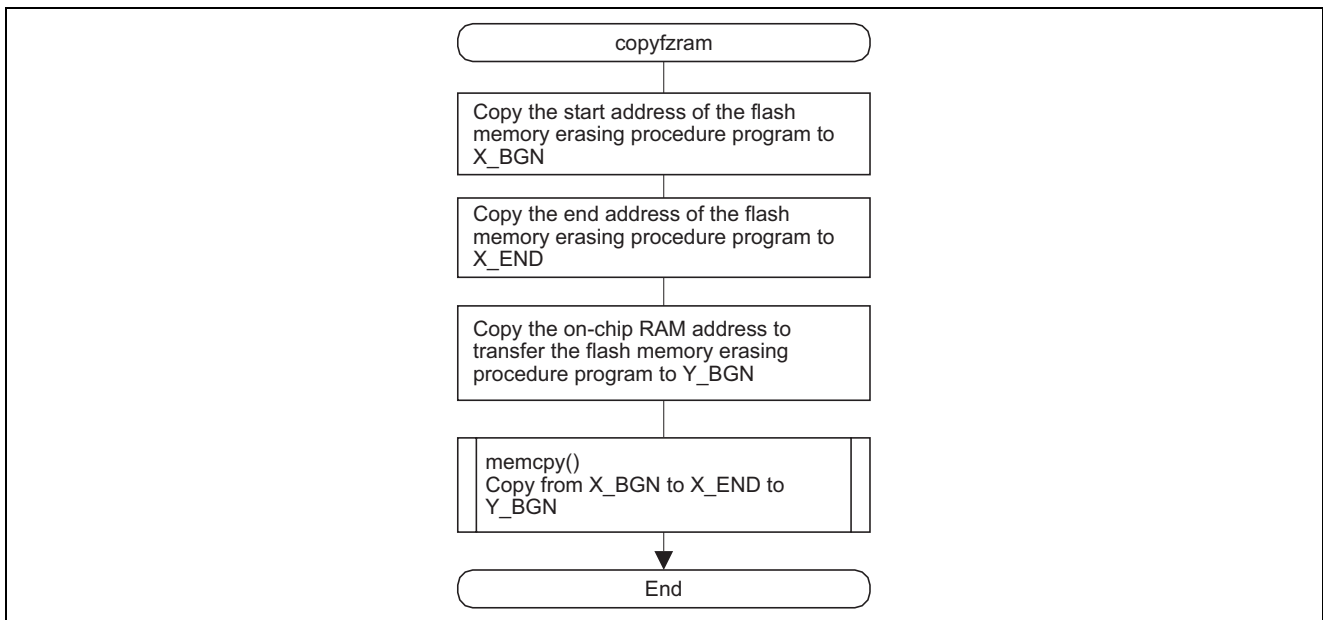
3. Return value

None

4. Description of internal registers used

None

5. Flowchart



5.5 Description of Functions for the Flash-Memory Erasure Procedure Program

5.5.1 flew_main Function

1. Functional overview
Main routine of the flash-memory erasure procedure program
2. Arguments
None
3. Return value

Type	Description
unsigned char	Error status

4. Description of internal registers used

The internal registers used in this sample task are listed below. Note that the settings shown below are for this sample task and are not initial values.

- Flash erase code select register (FECS) Number of bits: 8 Address: H'FFFFC6

Bit	Bit Name	Setting	R/W	Function
0	EPVB	1	R/W	Erase Pulse Verify Block Selects the erasing program. 0: On-chip erasing program is not selected. [Clear condition] Completion of transfer 1: On-chip erasing program is selected.

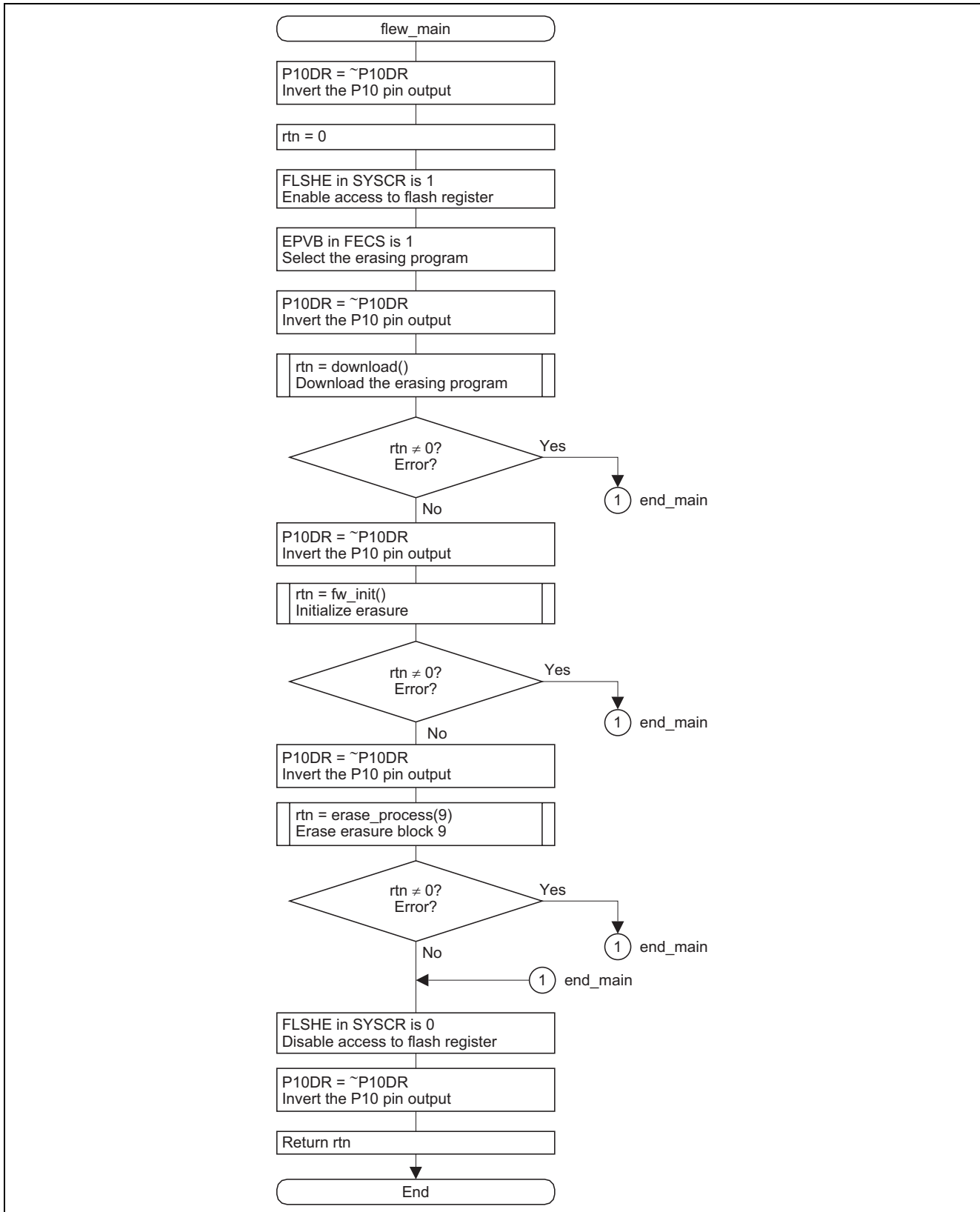
- Port 1 data register (P1DR) Number of bits: 8 Address: H'FFFF60

Bit	Bit Name	Setting	R/W	Function
0	P10DR	0/1	R/W	0: The P10 pin is low. 1: The P10 pin is high.

- System control register (SYSCR) Number of bits: 8 Address: H'FFFF3D

Bit	Bit Name	Setting	R/W	Function
3	FLSHE	0/1	R/W	Flash-Memory Control Register Enable Controls CPU access to the flash-memory control registers. If this bit is set to 1, the flash-memory control registers can be read from and written to. If this bit is cleared to 0, the flash-memory control registers are not selected. At this time, the contents of the flash-memory control registers are maintained. This bit should be written to 0 in other than flash-memory version. 0: Flash-memory control registers are not selected for area H'FFFFC4 to H'FFFFCF 1: Flash-memory control registers are selected for area H'FFFFC4 to H'FFFFCF

5. Flowchart



5.5.2 download Function

1. Functional overview

This function downloads the on-chip erasing program.

2. Arguments

None

3. Return value

Type	Description
unsigned char	Download pass/fail result (DPFR) Return value of the download result

4. Description of internal registers used

The internal registers used in this sample task are listed below. Note that the settings shown below are for this sample task and are not initial values.

- Flash key code register (FKEY) Number of bits: 8 Address: H'FFFFC8

Bit	Bit Name	Setting	R/W	Function
7	K7	1	R/W	Key Code
6	K6	0	R/W	When H'A5 is written to FEKY, writing to the SCO bit in FCCS is valid. When the value other than H'A5 is written to FKEY, 1 cannot be written to the SCO bit. Therefore downloading to the on-chip RAM cannot be executed. Only when H'5A is written, programming/erasing can be executed. Even if the on-chip programming/erasing program is executed, the flash memory cannot be programmed or erased when the value other than H'5A is written to FKEY. H'A5: Writing to the SCO bit is enabled (The SCO bit cannot be set by the value other than H'A5.) H'5A: Programming/erasing is enabled (The value other than H'A5 is in software protection state.) H'00: Initial value
5	K5	1	R/W	
4	K4	0	R/W	
3	K3	0	R/W	
2	K2	1	R/W	
1	K1	0	R/W	
0	K0	1	R/W	

• Flash transfer destination address register (FTDAR) Number of bits: 8 Address: H'FFFFCA

Bit	Bit Name	Setting	R/W	Function
7	TDER	0	R/W	<p>Transfer Destination Address Setting Error</p> <p>This bit is set to 1 when the address specified by bits TDA6 to TDA0, which is the start address to download an on-chip program, is over the range. Whether or not the range specified by bits TDA6 to TDA0 is within the range of H'00 to H'03 is determined when an on-chip program is downloaded by setting the SCO bit in FCCS. Make sure that this bit is cleared to 0 before setting the SCO bit to 1 and the value specified by TDA6 to TDA0 is within the range of H'00 to H'03.</p> <p>0: The value specified by bits TDA6 to TDA0 is within the range. 1: The value specified by is TDA6 to TDA0 is over the range (H'04 to H'FF) and the download is stopped.</p>
6	TDA6	0	R/W	Transfer Destination Address
5	TDA5	0	R/W	Specifies the start address to download. H'00 to H'03 can be specified meaning that the start address in the on-chip RAM space can be specified in units of 4 KB. H'00: Sets the address where downloading starts to H'FF9000. H'01: Sets the address where downloading starts to H'FFA000. H'02: Sets the address where downloading starts to H'FFB000. H'03: Sets the address where downloading starts to H'FF8000. H'04 to H'7F: Setting prohibited. Specifying this value sets the TDER bit to 1 and stops the download.
4	TDA4	0	R/W	
3	TDA3	0	R/W	
2	TDA2	0	R/W	
1	TDA1	0	R/W	
0	TDA0	0	R/W	

• Flash code control and status register (FCCS) Number of bits: 8 Address: H'FFFFC4

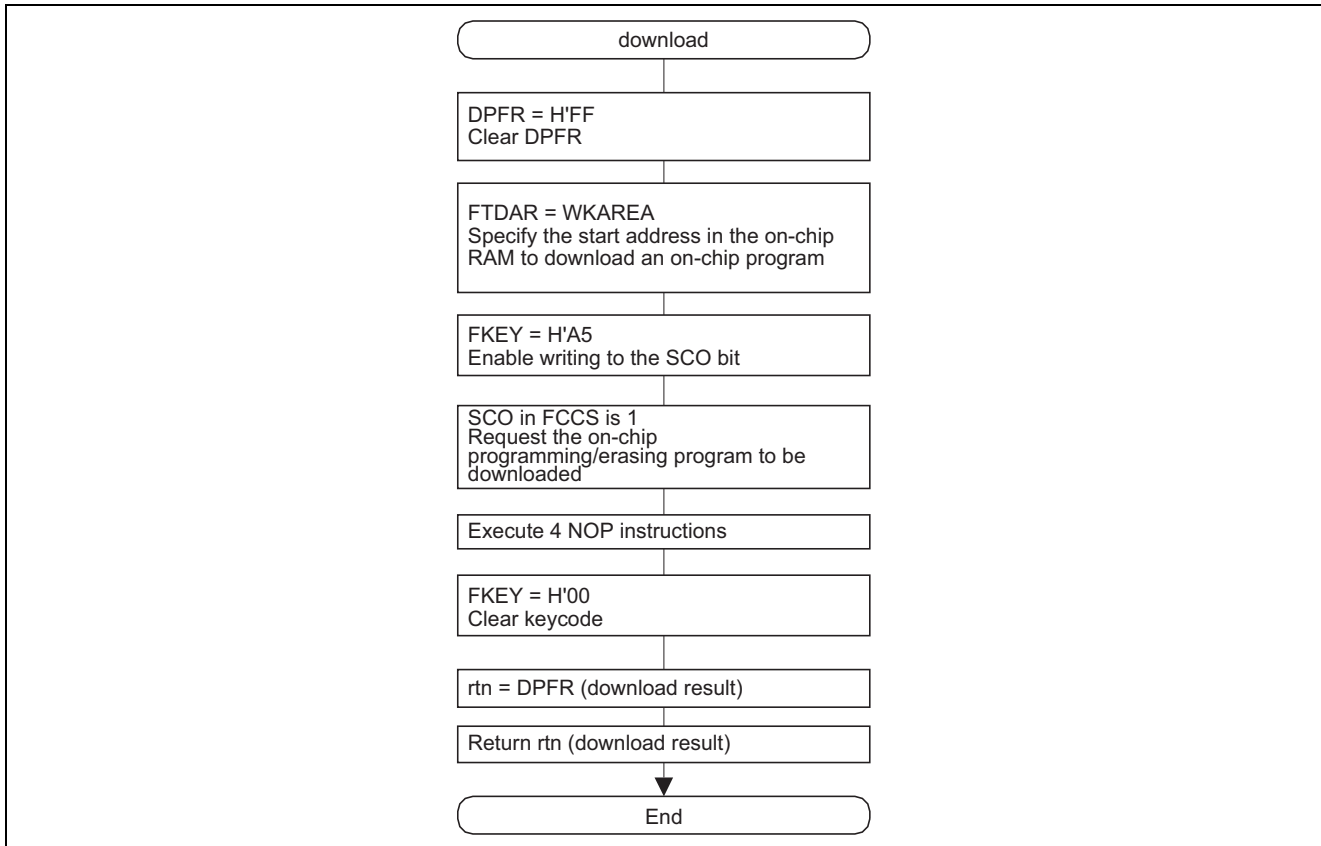
Bit	Bit Name	Setting	R/W	Function
4	FLER	—	R	<p>Flash-Memory Error</p> <p>Indicates an error occurs during programming and erasing flash memory. When FLER is set to 1, flash memory enters the error protection state. This bit is initialized at transition to a power-on reset or hardware standby mode. When FLER is set to 1, high voltage is applied to the internal flash memory. To reduce the damage to flash memory, the reset must be released after the reset period of 100 μs which is longer than normal.</p> <p>0: Flash memory operates normally. Programming/erasing protection for flash memory (error protection) is invalid. [Clearing condition] At a power-on reset or in hardware standby mode</p> <p>1: Indicates an error occurs during programming/erasing flash memory. Programming/erasing protection for flash memory (error protection) is valid. [Setting condition]</p> <ul style="list-style-type: none"> • Occurrence of an interrupt, such as NMI during programming/erasing flash memory • Reading of the flash memory during programming/erasing flash memory (including a vector read or an instruction fetch) • Execution of the SLEEP instruction during programming/erasing flash memory • Obtainment of bus mastership by a bus master other than the CPU, such as the DMAC, DTC, or BREQ during programming/erasing flash memory
0	SCO	0	(R)/W	<p>Source Program Copy Operation</p> <p>Requests the on-chip programming/erasing program to be downloaded to the on-chip RAM. When this bit is set to 1, the on-chip program which is selected by FPCS/FECS is automatically downloaded in the on-chip RAM specified by FTDAR. In order to set this bit to 1, H'A5 must be written to FKEY, and this operation must be executed in the on-chip RAM.</p> <p>Four NOP instructions must be executed immediately after setting this bit to 1. Since this bit is cleared to 0 when download is completed, this bit cannot be read as 1. All interrupts must be disabled. This should be made in the user system.</p> <p>0: Download of the on-chip programming/erasing program to the on-chip RAM is not executed [Clear condition] Completion of download</p> <p>1: Request for downloading of the on-chip programming/erasing program to the on-chip RAM has been issued [Setting condition] Writing of 1 to this bit while both of the following conditions are satisfied</p> <ol style="list-style-type: none"> (1) Writing of H'A5 to FKEY (2) Execution from the on-chip RAM is in progress.

- Download pass/fail result parameter (DPFR)
 (Single byte of start address specified by FTDAR)

This parameter indicates the return value of the download result. The value of DPFR can be used to determine if downloading is executed or not.

Bit	Bit Name	Setting	R/W	Function
2	SS	—	R/W	<p>Source Select Error Detect</p> <p>Only one type for the on-chip program which can be downloaded can be specified. When more than two types of the program are selected, the program is not selected, or the program is selected without mapping, error is occurred.</p> <p>0: Download program can be selected normally</p> <p>1: Download error is occurred (multi-selection or program which is not mapped is selected)</p>
1	FK	—	R/W	<p>Flash Key Register Error Detect</p> <p>Returns the check result whether the value of FKEY is set to H'A5.</p> <p>0: KEY setting is normal (FKEY = H'A5)</p> <p>1: Setting value of FKEY becomes error (FKEY = value other than H'A5)</p>
0	SF	—	R/W	<p>Success/Fail</p> <p>Returns the result whether download is ended normally or not. The determination result whether program that is downloaded to the on-chip RAM is read back and then transferred to the on-chip RAM is returned.</p> <p>0: Downloading on-chip program is ended normally (no error)</p> <p>1: Downloading on-chip program is ended abnormally (error occurs)</p>

5. Flowchart



5.5.3 fw_init Function

1. Functional overview

Initialization for flash-memory erasure processing

This function set the FPEFEQ and FUBRA parameters.

2. Arguments

None

3. Return value

Type	Description
unsigned char	Flash pass/fail parameter (FPFR) Return value of the initialization result

4. Description of internal registers used

The internal registers used in this sample task are listed below. Note that the settings shown below are for this sample task and are not initial values.

- Flash programming/erasing frequency parameter (FPEFEQ)
(General register ER0 of CPU)

This parameter sets the operating frequency of the CPU and enables the user branch function.

Bit	Bit Name	Setting	R/W	Function
31 to 16	FUBE15 to 0	H'AA55	R/W	Flash User Branch Enable Bit Set to H'AA55 if the user branch function is enabled. Otherwise, set to H'0000.
15 to 0	F15 to F0	CLOCK	R/W	Frequency Set Set the operating frequency of the CPU. When using the frequency multiplication factor of the PLL, set the frequency obtained by the multiplication. The setting value must be calculated as the following methods. <ul style="list-style-type: none"> The operating frequency which is shown in MHz units must be rounded in a number to three decimal places and be shown in a number of two decimal places. The value multiplied by 100 is converted to the binary digit and is written to the FPEFEQ parameter (general register ER0). For example, when the operating frequency of the CPU is 35.000 MHz, the value is as follows. <ol style="list-style-type: none"> The number to three decimal places of 35.000 is rounded and the value is thus 35.00. The formula that $35.00 \times 100 = 3500$ is converted to the binary digit and B'0000, 1101, 1010, 1100 (H'0CE4) is set to ER0.

- Flash user branch address setting parameter (FUBRA)
(General register ER1 of CPU)

This parameter sets the user branch destination address. A specified user routine can be used to perform programming or erasing of processing units of predetermined size. When using the user branch function, set the flash user branch enable bits in FPEFEQ to H'AA55 in addition to the settings in this register.

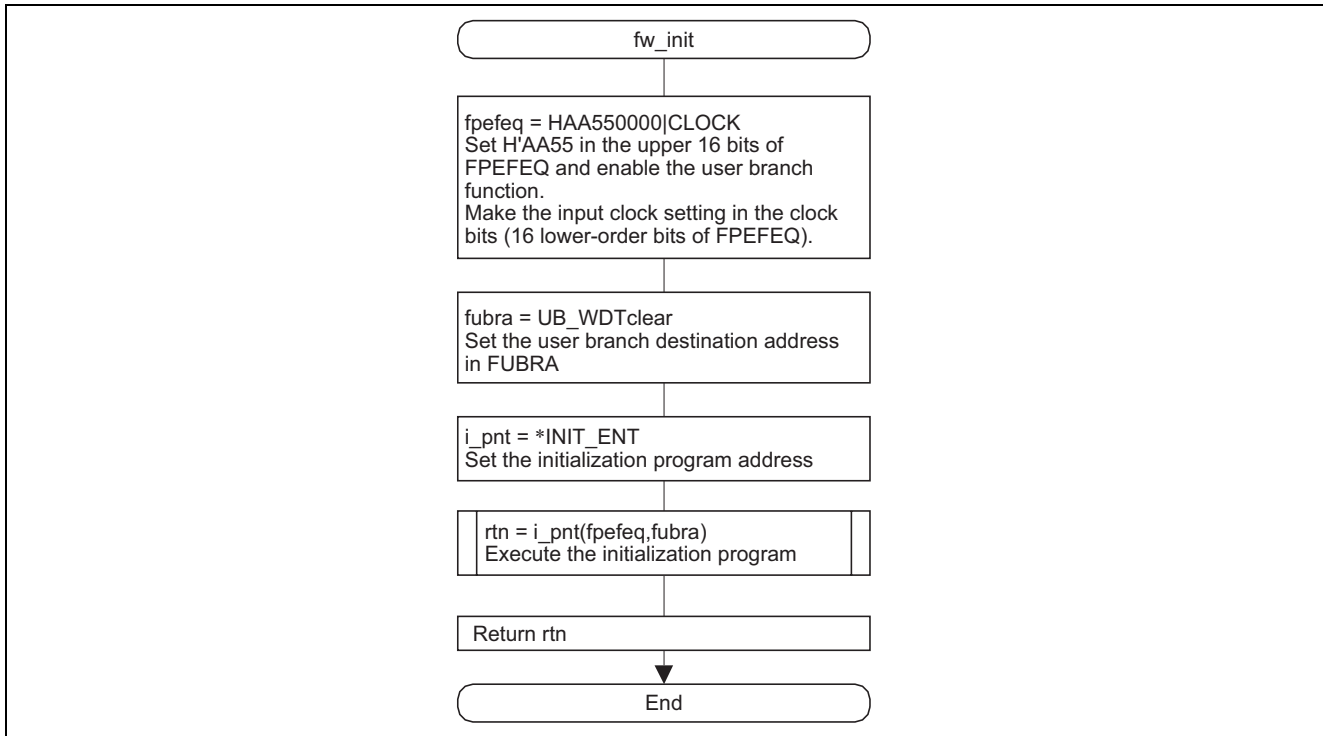
Bit	Bit Name	Setting	R/W	Function
31 to 0	UA31 to UA0	Start address of the UB_WDTclear function	R/W	<p>User branch destination address</p> <p>The user branch destination should be located in a space in RAM other than that to which internal programs are transferred or the external bus space.</p> <p>Be careful not to cause program runaway by branching to an area without execution codes, and do not destroy an area to which internal programs are downloaded or a stack area. The contents of flash memory cannot be guaranteed if program runaway occurs or if download or stack areas are destroyed.</p> <p>The user branch destination processing should not initiate downloading of internal programs, initialization, programming, or erasing. Programming or erasing cannot be guaranteed when returning from the user branch destination. Also, take care not to rewrite previously prepared programming data.</p> <p>Furthermore, do not rewrite program/erase interface registers as part of the user branch destination processing. After user branch processing completes, use the RTS instruction to return to the program/erase program.</p>

- Flash pass/fail parameter (FPFR)
(General register R0L of CPU)

This parameter indicates the return value of the initialization result.

Bit	Bit Name	Setting	R/W	Function
2	BR	—	R/W	<p>User Branch Error Detect</p> <p>Returns the check result whether the specified user branch destination address is in the area other than the storage area of the programming/erasing program which has been downloaded.</p> <p>0: User branch address setting is normal 1: User branch address setting is abnormal</p>
1	FQ	—	R/W	<p>Frequency Error Detect</p> <p>Returns the check result whether the specified operating frequency of the CPU is in the range of the supported operating frequency.</p> <p>0: Setting of operating frequency is normal 1: Setting of operating frequency is abnormal</p>
0	SF	—	R/W	<p>Success/Fail</p> <p>Indicates whether initialization is completed normally.</p> <p>0: Initialization is ended normally (no error) 1: Initialization is ended abnormally (error occurs)</p>

5. Flowchart



5.5.4 erase_process Function

1. Functional overview

Flash-memory erasure processing

2. Argument

Type	Variable Name	Description
unsigned long	febs	Erase-block number

3. Return value

Type	Description
unsigned char	Flash pass/fail parameter (FPFR) Return value of the erasing processing result

4. Description of internal registers used

The internal registers used in this sample task are listed below. Note that the settings shown below are for this sample task and are not initial values.

- Flash key code register (FKEY) Number of bits: 8 Address: H'FFFFC8

Bit	Bit Name	Setting	R/W	Function
7	K7	0	R/W	Key Code
6	K6	1	R/W	When H'A5 is written to FKEY, writing to the SCO bit in FCCS is valid. When the value other than H'A5 is written to FKEY, 1 cannot be written to the SCO bit. Therefore downloading to the on-chip RAM cannot be executed.
5	K5	0	R/W	
4	K4	1	R/W	
3	K3	1	R/W	Only when H'5A is written, programming/erasing can be executed. Even if the on-chip programming/erasing program is executed, the flash memory cannot be programmed or erased when the value other than H'5A is written to FKEY.
2	K2	0	R/W	
1	K1	1	R/W	H'A5: Writing to the SCO bit is enabled (The SCO bit cannot be set by the value other than H'A5.) H'5A: Programming/erasing is enabled (any value other than H'A5 places the flash memory in the software-protection state.)
0	K0	0	R/W	

H'00: Initial value

- Flash pass/fail parameter (FPFR)
(General register R0L of CPU)

This parameter returns value of the erasing processing result.

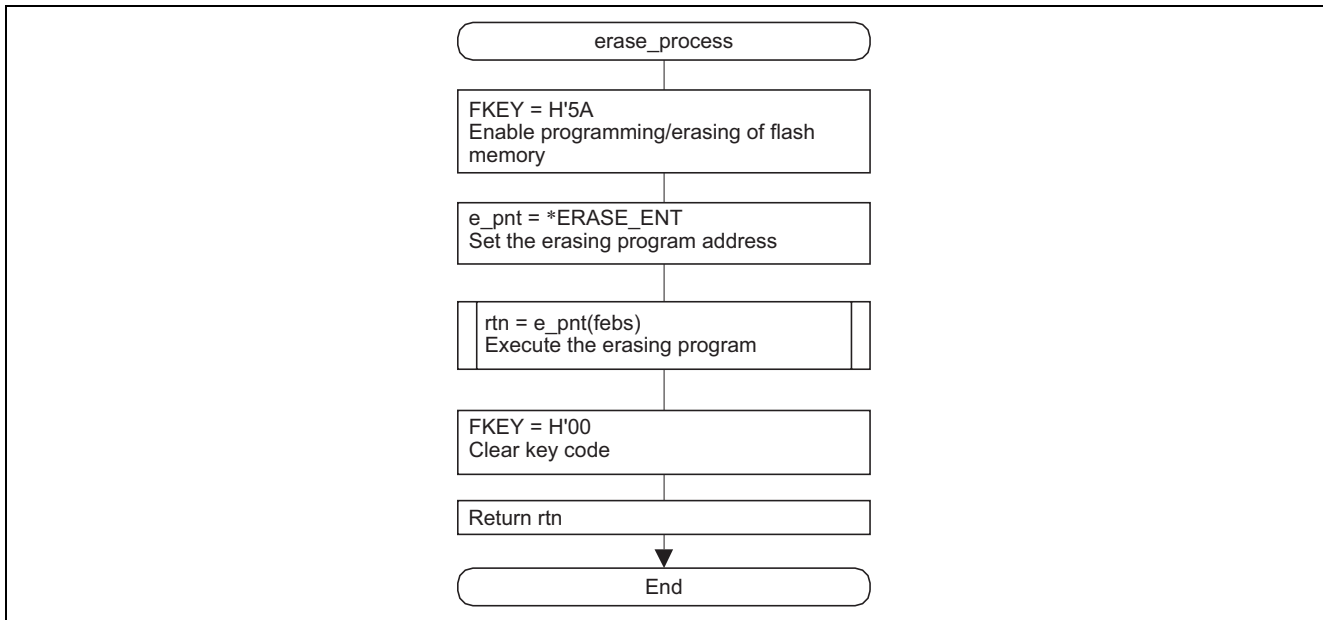
Bit	Bit Name	Setting	R/W	Function
6	MD	—	R/W	Erasing Mode Related Setting Error Detect Returns the check result of whether the error protection state is entered. When the error protection state is entered, 1 is written to this bit. The error protection state can be confirmed with the FLER bit in FCCS. 0: FLER setting is normal (FLER = 0) 1: FLER = 1 and erasing cannot be performed
5	EE	—	R/W	Erasure Execution Error Detect 1 is returned to this bit when the user MAT could not be erased or when flash-memory related register settings are partially changed on returning from the user branch processing. If this bit is set to 1, there is a high possibility that the user MAT is partially erased. In this case, after removing the error factor, erase the user MAT. If FMATS is set to H'AA and the user boot MAT is selected, an error occurs when erasure is performed. In this case, both the user MAT and user boot MAT are not erased. Erasing of the user boot MAT should be performed in boot mode or PROM mode.
4	FK	—	R/W	Flash Key Register Error Detect Returns the check result of FKEY value before start of the erasing processing. 0: FKEY setting is normal (FKEY = H'5A) 1: FKEY setting is error (FKEY = value other than H'5A)
3	EB	—	R/W	Erase Block Select Error Detect Returns the check result whether the specified erase-block number is in the block range of the user MAT. 0: Setting of erase-block number is normal 1: Setting of erase-block number is abnormal
0	SF	—	R/W	Success/Fail Indicates whether the erasing processing is ended normally or not. 0: Erasure is ended normally (no error) 1: Erasure is ended abnormally (error occurs)

- Flash erase block select parameter (FEBS)
(General register ER0 of CPU)

This parameter specifies the erase-block number

Bit	Bit Name	Setting	R/W	Function
7 to 0	EBN7 to 0	febs	R/W	Erase Block Number Set an erase-block number within the range from 0 to 15. H'00 corresponds to the EB0 block and H'0F corresponds to the EB15 block. An error occurs if a number outside the range from H'00 to H'0F is set.

5. Flowchart



5.5.5 UB_WDTclear Function

1. Functional overview

User branch processing. This is the user processing routine at the user branch destination, i.e. the function that produces WDT-clearing signals on the P10 pin.

2. Arguments

None

3. Return value

Type	Description
unsigned char	Flash pass/fail parameter (FPFR) Return value of the initialization result

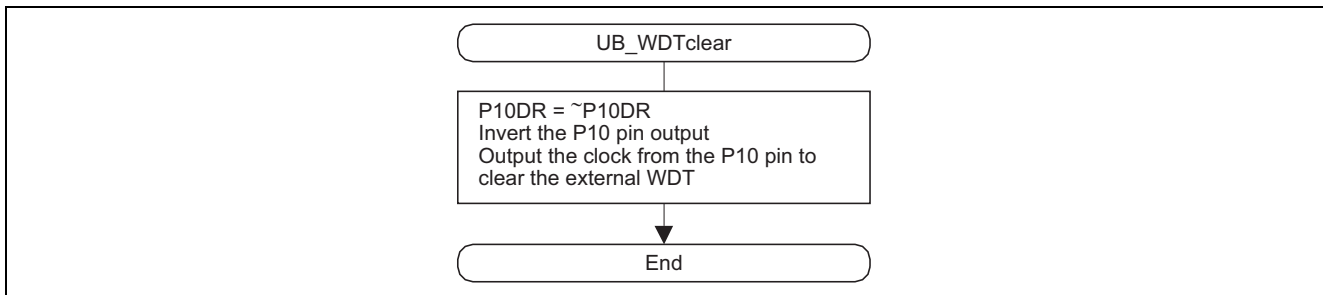
4. Description of internal registers used

The internal registers used in this sample task are listed below. Note that the settings shown below are for this sample task and are not initial values.

- Port 1 data register (P1DR) Number of bits: 8 Address: H'FFFF60

Bit	Bit Name	Setting	R/W	Function
0	P10DR	0/1	R/W	0: The P10 pin is low. 1: The P10 pin is high.

5. Flowchart



6. Documents for Reference

- Hardware Manual
H8S/2378 and H8S/2378R Group Hardware Manuals
The most up-to-date versions of these documents are available on the Renesas Technology Website.
- Technical News/Technical Update
The most up-to-date information is available on the Renesas Technology Website.

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.07.08	—	First edition issued

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