

---

# RX62N Group, RX621 Group

## 32-Bit SDRAM Connection and Access

---

R01AN0585EJ0100  
Rev.1.00  
Oct 28, 2011

### Introduction

This application note presents a sample application in which an RX62N Group or RX621 Group microcontroller is connected to and accesses 32-bit SDRAM.

### Corresponding Device

RX62N Group and RX621 Group devices

The sample application presented here can also be used with other RX Family devices that have the same I/O registers (peripheral function control registers) as the RX62N Group and RX621 Group devices. Note, however, that since certain peripheral functions have added functionality, the manual must be checked for compatibility. If this application note's content is used in an application, it's operation must be fully evaluated before deployment.

### Contents

1. Specifications .....	2
2. Operation Verification Environment .....	3
3. Functions Used .....	3
4. Operation.....	4
5. Software .....	12
6. Reference Documents.....	22

### 1. Specifications

The SDRAM interface included in the RX62N Group and RX621 Group devices can directly connect with up to 128 MB (1024 Mbit) of SDRAM and supports SDRAM devices with a CAS latency of from 1 to 3 cycles.

This sample application uses an RX62N and a 128 Mbit SDRAM (Micron MT48LC4M32B2P-7: 1 Mword × 32 bits × 4 banks) connected by a 32-bit bus.

Figure 1 presents an SDRAM connection circuit example. Table 1 lists the SDRAM specifications.

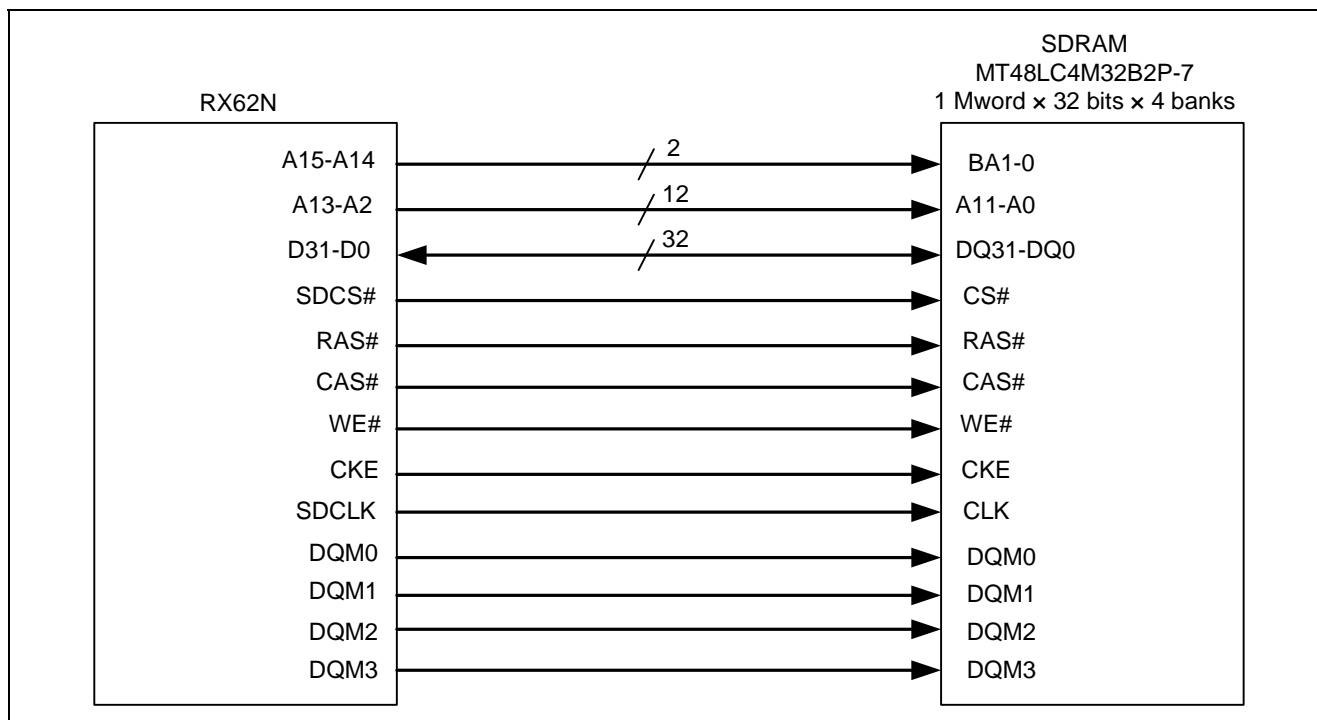


Figure 1 32-bit SDRAM Connection

Table 1 SDRAM Specifications

Item	Symbol	Description
Product name	—	Micron MT48LC4M32B2P-7
Structure	—	1 Mword × 32 bits × 4 banks
Capacity	—	1024 Mbits
Row address lines	—	A11-A0
Column address lines	—	A7-A0
Auto-refresh interval	—	4096 refresh cycles every 64 ms
CAS latency	—	1/2/3
Number of initialization auto-refresh operations	—	Two
Auto-refresh period	(tRFC)	70 ns (min)
Precharge period	(tRP)	20 ns (min)
Write recovery period	(tWR)	14 ns (min)
Precharge command period	(tRP)	20 ns (min)
Active command to precharge command period	(tRAS)	42 ns (min)
Active command to read or write command delay time	(tRCD)	20 ns (min)

## 2. Operation Verification Environment

Table 2 lists the environment used to verify the operation described in this document.

**Table 2 Operation Verification Environment**

Item	Description
Device	RX62N (R5F562N8BDBG)
Board	RSK RX62N (R0K5562N0C010BR)
Supply voltage	3.3 V (Supplied from E1)
Input clock	12 MHz (ICLK = 96 MHz, PCLK = 48 MHz, BCLK/SDCLK = 48 MHz)
Operating temperature	Room temperature
HEW	Version 4.09.00.007
Toolchain	RX Standard Toolchain (V.1.0.0.0)
Debugger/Emulator	E1 emulator
Debugger component	RX E1/E20 SYSTEM V.1.02.00.000

## 3. Functions Used

- Bus  
See the Hardware Manual listed in section 6, Reference Documents, for details.

## 4. Operation

### 4.1 SDRAM Initialization Sequence Settings

Initialization is required before accessing the SDRAM used. Applications should perform this initialization once after a reset. The initialization sequence must be performed in a manner that observes the initialization auto-refresh interval, initialization auto-refresh count, and the initialization precharge cycle specified in the datasheet for the SDRAM used. The following describes how to determine the corresponding setting values. Table 3 lists the values used in this sample application.

#### 1. Initialization auto-refresh interval

Since the SDRAM used in this sample application has an auto-refresh interval (tRFC) of 70 ns (minimum), the SDRAMC initialization auto-refresh interval must be set so that the following holds.

$$70 \text{ ns (minimum)} \leq \text{initialization auto-refresh interval}$$

Also, since the SDRAM clock (SDCLK) setting used in this application note is 48 MHz, the SDCLK period will be 1/48 MHz.

Therefore, since

$$70 \text{ ns (minimum)} / (1/48 \text{ MHz}) = 3.36 \text{ cycles,}$$

an initialization auto-refresh interval of at least 4 cycles is required.

Therefore the initialization auto-refresh interval field (ARFI[3:0]) is set to 0001b.

#### 2. Initialization auto-refresh count

The SDRAM used in this sample application requires an initialization auto-refresh to be performed twice.

Therefore the initialization auto-refresh count field (ARFC[3:0]) is set to 0010b.

#### 3. Initialization precharge cycles

Since the precharge command period (tRP) for the SDRAM used in this sample application is 20 ns (minimum), the following condition must be met.

$$20 \text{ ns (minimum)} \leq \text{initialization precharge count}$$

Since

$$20 \text{ ns} / (1/48 \text{ MHz}) = 0.96 \text{ cycles,}$$

at least one cycle is required for the SDRAM initialization precharge cycles. However, since it is not possible to set this value to less than 3 in the RX62N SDRAMC specifications, the set value used is 3 cycles.

Accordingly, the initialization precharge cycles field (PRC[2:0]) is set to 000b.

Table 3 SDRAM Initialization Auto-Refresh Control Register (SDIR)

Field Name	Setting Value	Function
Initialization auto-refresh interval (ARFI[3:0])	0001b	4 cycles
Initialization auto-refresh count (ARFC[3:0])	0010b	2 times
Initialization precharge cycle count setting (PRC[2:0])	000b	3 cycles

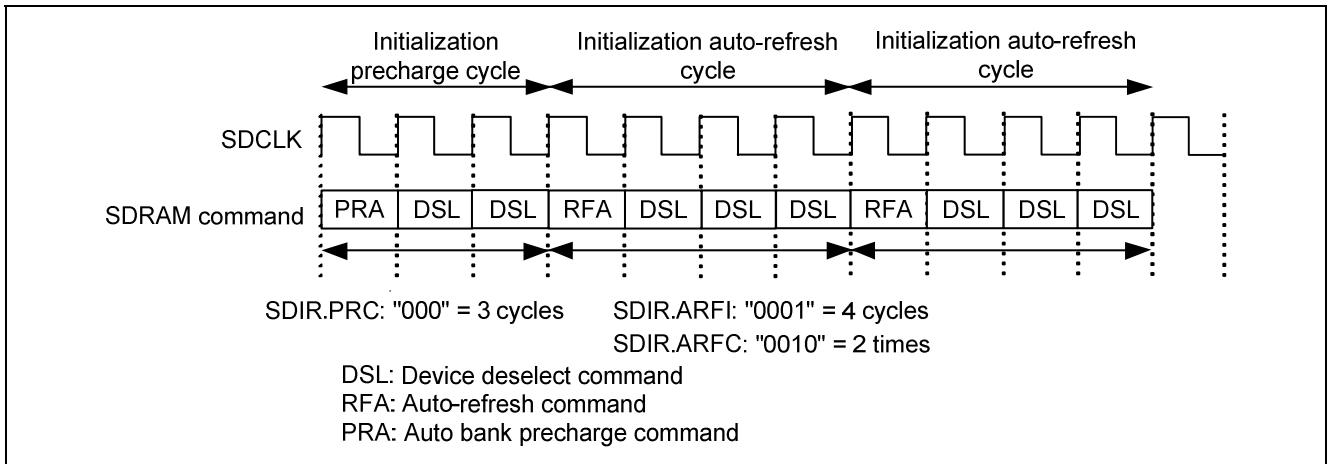


Figure 2 Initialization Sequence Timing

### 4.2 SDRAM Mode Register Settings

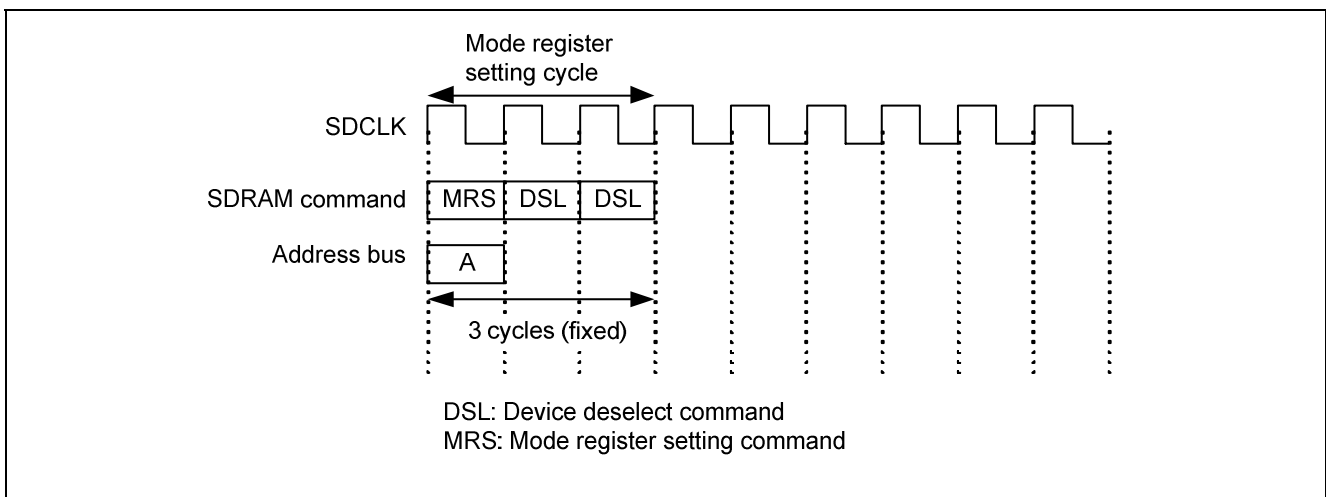
The SDRAM mode must be set after SDRAM initialization. Applications should only set the mode once after initialization. The SDRAM mode register can be written automatically by writing the value to the RX62N SDRAM controller's SDRAM mode register. Table 4 lists the values used in this sample application.

1. Mode register

The RX62N SDRAM controller operates with a burst length of 1. Operation is not guaranteed for an value other than a burst lengths of 1. This sample application operates with a burst length of 1, a column latency of 1 cycle, and in single access mode.

**Table 4 SDRAM Mode Register (SMOD)**

Field Name	Setting Value	Function
Mode register setting field (MR[14:0])	210h	Burst length: 1, Column latency: 1 cycle Single access mode



**Figure 3 SDRAM Mode Register Setting Timing**

### 4.3 Auto Refresh Settings

This sample application uses the SDRAM's auto-refresh function. Auto refresh must be performed while observing the auto-refresh request interval and the auto-refresh clear cycle specified in the datasheet for the SDRAM. The following describes how to determine the corresponding setting values. Table 5 lists the values used in this sample application.

#### 1. Auto-refresh request interval

The following formula can be used to determine the auto-refresh request interval.

$$\text{RFC (auto-refresh request interval setting value)} = (\text{auto-refresh request interval}/\text{SDCLK period}) - 1$$

Since the SDRAM used in this sample application requires that auto refresh be performed 4096 times every 64 ms, this interval is determined as follows.

$$\text{auto-refresh request interval} = 64 \text{ ms}/4096 = 15.625 \text{ } \mu\text{s}$$

Also, since the SDRAM clock (SDCLK) setting used in this application note is 48 MHz, the SDCLK period will be 1/48 MHz.

Therefore, the RFC value is calculated as follows.

$$\begin{aligned} \text{RFC (auto-refresh request interval setting value)} &= (15.625 \text{ } \mu\text{s}/(1/48 \text{ MHz})) - 1 \\ &= 749 \\ &= 2\text{EDh} \end{aligned}$$

Accordingly the auto-refresh request interval field (RFC[11:0]) is set to 2EDh.

#### 2. Auto-refresh clear cycle

Since the SDRAM used in this sample application has an auto-refresh clear cycle (tRFC) of 70 ns (minimum), the SDRAMC auto-refresh clear cycle must be set so that the following holds.

$$70 \text{ ns (minimum)} \leq \text{initialization auto-refresh interval}$$

Therefore, since

$$70 \text{ ns (minimum)}/(1/48 \text{ MHz}) = 3.36 \text{ cycles,}$$

an auto-refresh clear cycle count of at least 4 is required.

Therefore the initialization auto-refresh clear cycle field (REFW[3:0]) is set to 0011b.

**Table 5 SDRAM Auto-Refresh Control Register (SDRFCR)**

Field Name	Setting Value	Function
Auto-refresh request interval setting field (RFC[11:0])	02EDh	749 cycles
Auto-refresh cycle/self-refresh clear cycle count setting field (REFW[3:0])	0011b	4 cycles

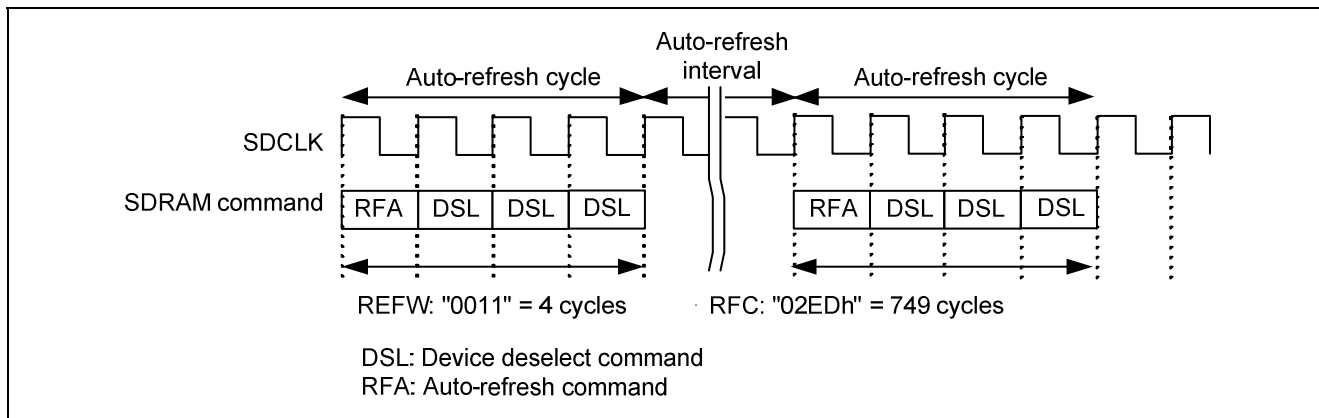


Figure 4 Auto-Refresh Timing

## 4.4 SDRAM Timing Settings

This sample application sets the access timing according to the specifications of the SDRAM used. In particular, the SDRAM must be accessed while observing the access timing listed in the SDRAM datasheet. The following describes how to determine the corresponding setting values. Table 6 lists the values used in this sample application.

### 1. SDRAM controller column latency setting

Since this sample application can operate with a CAS latency of from 1 to 3, it uses a CAS latency of 1 cycle.

Accordingly, the SDRAMC column latency setting field (CL[2:0]) is set to 001b.

### 2. Write recovery period setting

Since the write recovery period (tWR) for the SDRAM used in this sample application is 14 ns (minimum), the SDRAM controller write recovery period must meet the following condition.

$$14 \text{ ns (minimum)} \leq \text{write recovery period}$$

Since

$$14 \text{ ns}/(1/48 \text{ MHz}) = 0.672 \text{ cycles,}$$

a write recovery period of at least 1 cycle is required.

Accordingly, the write recovery period setting field (WR) is set to 0b.

### 3. Row precharge period setting

Since the precharge command period (tRP) for the SDRAM used in this sample application is 20 ns (minimum), the SDRAM controller row precharge period must meet the following condition.

$$20 \text{ ns} \leq \text{row precharge period}$$

Since

$$20 \text{ ns}/(1/48 \text{ MHz}) = 0.96 \text{ cycles,}$$

a row precharge period of at least 1 cycle is required.

Accordingly, the row precharge period setting field (RP[2:0]) is set to 000b.

### 4. Row active period setting

The period from an active command to a precharge command (tRAS) for the SDRAM used in this sample application is 42 ns (minimum), the SDRAM controller row active period must meet the following condition.

$$42 \text{ ns (minimum)} \leq \text{row active period}$$

Since

$$42 \text{ ns}/(1/48 \text{ MHz}) = 2.016 \text{ cycles,}$$

a row active period of at least 3 cycles is required.

Accordingly, the row active period setting field (RAS[2:0]) is set to 010b.

Note that the SDRAM controller row active period setting field value must meet the following stipulation.

$$\text{Row active period} \leq (\text{row column latency}) + \text{SDRAM controller column latency}$$

## 5. Row column latency setting

Since the delay time from the point an active command is issued until a read or write command is issued for the SDRAM used in this sample application is 20 ns (minimum), the SDRAM controller row column latency must meet the following condition.

$$20 \text{ ns} \leq \text{row column latency}$$

Since

$$20 \text{ ns}/(1/48 \text{ MHz}) = 0.96 \text{ cycles},$$

a row column latency of at least 1 cycle is required.

However, the SDRAM controller row active period setting field value must meet the following stipulation.

$$\text{Row active period} \leq (\text{row column latency}) + \text{SDRAM controller column latency}$$

Since

$$\text{Row active period} = 3 \text{ cycles}$$

and

$$\text{SDRAM controller column latency} = 1 \text{ cycle},$$

This means that

$$\begin{aligned} \text{The set number of cycles for the row column latency} &\geq (3 \text{ cycles}) - (1 \text{ cycle}) \\ &\geq 2 \text{ cycles}. \end{aligned}$$

Thus the row column latency must be set to at least 2 cycles.

Accordingly, the row column latency setting field (RCD[1:0]) is set to 01b.

Table 6 SDRAM Timing Register (SDTR)

Bit Name	Setting Value	Function
SDRAMC column latency setting field (CL[2:0])	001b	1 cycle
Write recovery period setting bit (WR)	0b	1 cycle
Row precharge period setting field (RP[2:0])	000b	1 cycle
Row active period setting field (RAS[2:0])	010b	3 cycles
Row column latency setting field (RCD[1:0])	01b	2 cycles

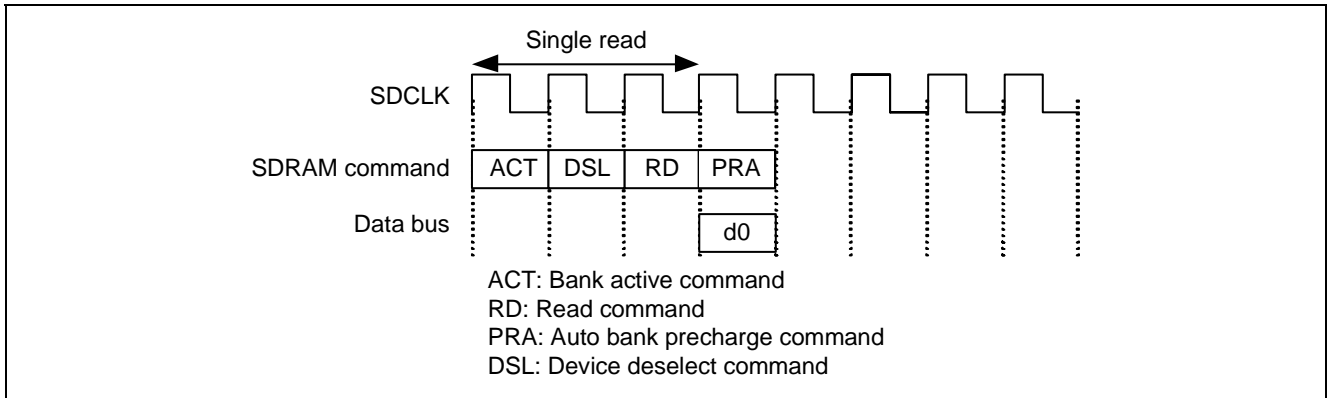


Figure 5 Read Timing

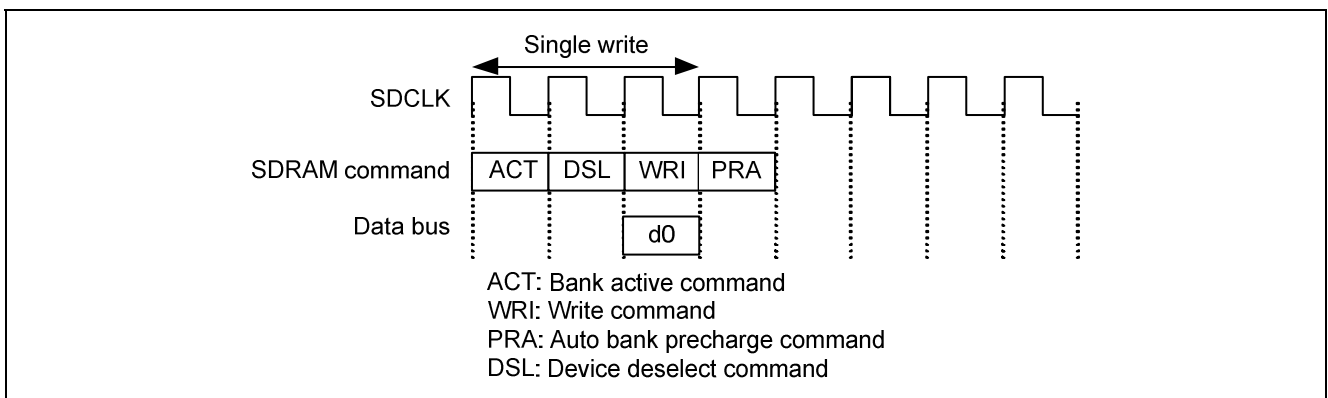


Figure 6 Write Timing

## 5. Software

### 5.1 Symbolic Constants

**Table 7 Symbolic Constants**

Constant	Value	Description	Functions
sdram_top	0x08000000	SDRAM (32-bit) start address	main
sdram_end	0x09000000	SDRAM (32-bit) end address	main

### 5.2 RAM Variables

**Table 8 RAM Variables**

Constant	Variables	Description	Functions
Unsigned long	sdram_adr	SDRAM (32-bit) address pointer	main
Unsigned long	sdram_data	SDRAM (32-bit) data variable	main
Unsigned long	sdram_cmp_data	SDRAM (32-bit) comparison data	main

### 5.3 Functions

**Table 9 Functions**

Function	Description
PowerON_Reset_PC	Initialization function Sets INTB, FPSW, and PSW, changes the processor mode, and calls main().
Main	Main function Calls the init() function, performs the program operations (reading and writing SDRAM), and calls the err() function.
Init	Microcontroller initialization function Sets various registers.
Err	Error function Handles SDRAM data compare check errors.

## 5.4 I/O Registers Used in this Application

The I/O registers shown below are used by this sample application. Note that the values shown are the values used in this sample application, not the initial values.

### (1) Clock generation circuit

System Clock Control Register (SCKCR)

Number of bits: 32, Address: 0008 0020h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b11 to b8	PCK[3:0]	0001	Peripheral module clock select bit	0001: × 4 PCLK = 48 MHz (When the EXTAL clock frequency is 12 MHz.)	R/W
b19 to b16	BCK[3:0]	0010	External bus clock, SDRAM select bit	0001: × 4 BCLK, SDCLK = 48 MHz (When the EXTAL clock frequency is 12 MHz.)	R/W
b22	PSTOP0	0	SDCLK pin output control bit	0: SDCLK pin output operates	R/W
b27 to b24	ICK[3:0]	0000	System clock select bit	0000: × 8 ICLK = 96 MHz (When the EXTAL clock frequency is 12 MHz.)	R/W

### (2) Operating mode

System Control Register 0 (SYSCR0)

Number of bits: 8, Address: 0008 0006h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b0	ROME	1	Internal ROM enable bit	1: Internal ROM enabled	R/W
b1	EXBE	1	External bus enable bit	1: External bus enabled	R/W
b15 to b8	KEY[7:0]	5Ah	SYSCR0 queue code	5Ah: SYSCR0 register write enabled	R/W

## (3) I/O ports

Port Function Register 3 (PF3BUS)

Number of bits: 8, Address: 0008 C103h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b0	A16E	0	Address A16 output enable bit	0: A16 output disabled	R/W
b1	A17E	0	Address A17 output enable bit	0: A17 output disabled	R/W
b2	A18E	0	Address A18 output enable bit	0: A18 output disabled	R/W
b3	A19E	0	Address A19 output enable bit	0: A19 output disabled	R/W
b4	A20E	0	Address A20 output enable bit	0: A20 output disabled	R/W
b5	A21E	0	Address A21 output enable bit	0: A21 output disabled	R/W
b6	A22E	0	Address A22 output enable bit	0: A22 output disabled	R/W
b7	A23E	0	Address A23 output enable bit	0: A23 output disabled	R/W

Port Function Register 4 (PF4BUS)

Number of bits: 8, Address: 0008 C104h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b1, 0	ADRLE[1:0]	11	Address low order A9 to A0 output enable bit	11: A9 to A0 output enabled	R/W
b2	A10E	1	Address low order A10 output enable bit	1: A10 output enabled	R/W
b3	A11E	1	Address low order A11 output enable bit	1: A11 output enabled	R/W
b4	A12E	1	Address low order A12 output enable bit	1: A12 output enabled	R/W
b5	A13E	1	Address low order A13 output enable bit	1: A13 output enabled	R/W
b6	A14E	1	Address low order A14 output enable bit	1: A14 output enabled	R/W
b7	A15E	1	Address low order A15 output enable bit	1: A15 output enabled	R/W

Port Function Register 5 (PF5BUS)

Number of bits: 8, Address: 0008 C105h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b4	DHE	1	Data D15 to D18 enable bit	1: PE7 to PE0 set to function as external data bus D15 to D8.	R/W
b5	DHE32E	1	Data D31 to D16 enable bit	1: PG7 to PG0 and P97 to P90 set to function as external data bus D31 to D16.	R/W

Port Function Register 6 (PF6BUS)

Number of bits: 8, Address: 0008 C106h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b4	MDSDE	1	SDRAM pin enable	See the description of the b6 (DQM1E bit).	R/W
b6	DQM1E	1	DQM1 enable	MDSDE, DQM1E 11: SDRAM enabled (all pins)	R/W
b7	SDCLKE	1	SDCLK enable	1: SDCLK output enabled	R/W

Data Register (PODR)

Number of bits: 8, Address: 0008 C020h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b2	B2	0	P02 output data storage bit	0: Output data = 0	R/W
b3	B3	0	P03 output data storage bit	0: Output data = 0	R/W

Data Direction Register (PODDR)

Number of bits: 8, Address: 0008 C000h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b2	B2	1	P02 input/output specification bit	1: Output port	R/W
b3	B3	1	P03 input/output specification bit	1: Output port	R/W

## (4) External bus

SDRAM Initialization Sequence Control Register (SDICR)

Number of bits: 8, Address: 0008 3C20h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b0	INIRQ	1	Initialization sequence start bit	1: Start initialization sequence	R/W

SDRAM Initialization Register (SDIR)

Number of bits: 16, Address: 0008 3C24h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b3 to b0	ARFI[3:0]	0001	Initialization auto-refresh interval bit	0001: 4 cycles	R/W
b7 to b4	ARFC[3:0]	0010	Initialization auto-refresh count bit	0010: Two times	R/W
b10 to b8	PRC[2:0]	000	Initialization precharge cycle count setting bit	000: 3 cycles	R/W

SDC Control Register (SDCCR)

Number of bits: 8, Address: 0008 3C00h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b0	EXENB	1	Operation enable bit	1: Operation enabled	R/W
b5, b4	BSIZE[1:0]	01	SDRAM bus width selection bit	01: Specifies use of a 32-bit bus space	R/W

SDRAM Mode Register (SDMOD)

Number of bits: 16, Address: 0008 3C48h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b14 to b0	MR[14:0]	0210h	Mode register setting bit	Write execution: issue mode register set command	R/W

SDRAM Refresh Control Register (SDRFRCR)

Number of bits: 16, Address: 0008 3C14h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b11 to b0	RFC[11:0]	2EDh	Auto-refresh request interval setting bit	001011101101: 749 cycles	R/W
b15 to b12	REFW[3:0]	0011	Auto-refresh cycle/self-refresh clear cycle count setting bit	0011: 4 cycles	R/W

SDRAM Auto-Refresh Control Register (SDRFEN)

Number of bits: 8, Address: 0008 3C16h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b0	RFEN	1	Auto-refresh operation enable bit	1: Auto refresh enabled	R/W

SDC Mode Register (SDCMOD)

Number of bits: 8, Address: 0008 3C01h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b0	EMODE	0	Endian specification bit	0: The same endian order as that of the operating mode is used as the SDRAM address space endian order.	R/W

SDRAM Access Mode Register (SDAMOD)

Number of bits: 8, Address: 0008 3C02h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b0	BE	0	Continuous access enable	0: Continuous access disabled	R/W

SDRAM Address Register (SDADR)

Number of bits: 8, Address: 0008 3C40h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b1, b0	MXC[1:0]	00	Address multiplexing selection bit	00: 8-bit shift	R/W

SDRAM Timing Register (SDTR)

Number of bits: 32, Address: 0008 3C44h

Bit	Symbol	Setting Value	Bit Name	Function	R/W
b2 to b0	CL[2:0]	001	SDRAMC column latency setting bit	001: 1 cycle	R/W
b8	WR	0	Write recovery period setting bit	0: 1 cycle	R/W
b11 to b9	RP[2:0]	000	Row precharge period setting bit	000: 1 cycle	R/W
b13, b12	RCD[1:0]	01	Row column latency setting bit	01: 2 cycles	R/W
b18 to b16	RAS[2:0]	010	Row active period setting bit	010: 3 cycles	R/W

## 5.5 Functions

### 5.5.1 PowerON\_Reset\_PC()

#### (1) Functional description

The PowerON\_Reset\_PC() function initializes the stack pointer (SP) and uses embedded functions and standard library functions to set interrupt mask bits, initialized/uninitialized data, and other items. It then calls the main() function.

#### (2) Arguments

None

#### (3) Return Values

None

#### (4) Flowchart

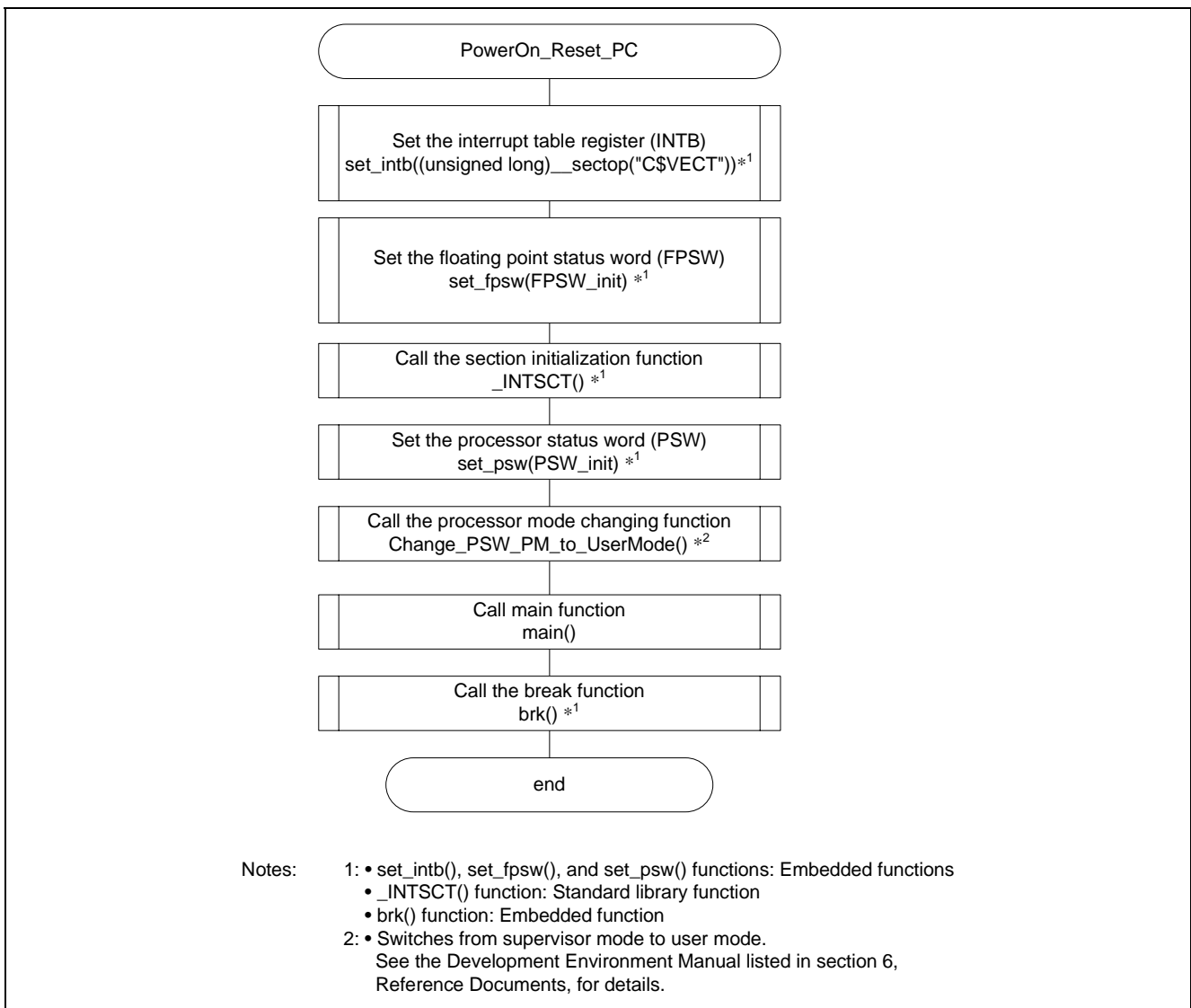


Figure 7 PowerON\_Reset\_PC() Function Flowchart

5.5.2 main() Function

(1) Functional description

The main() function calls the init() and err() functions and performs the sample program operations (memory reads and writes, and data comparisons).

(2) Arguments

None

(3) Return Values

None

(4) Flowchart

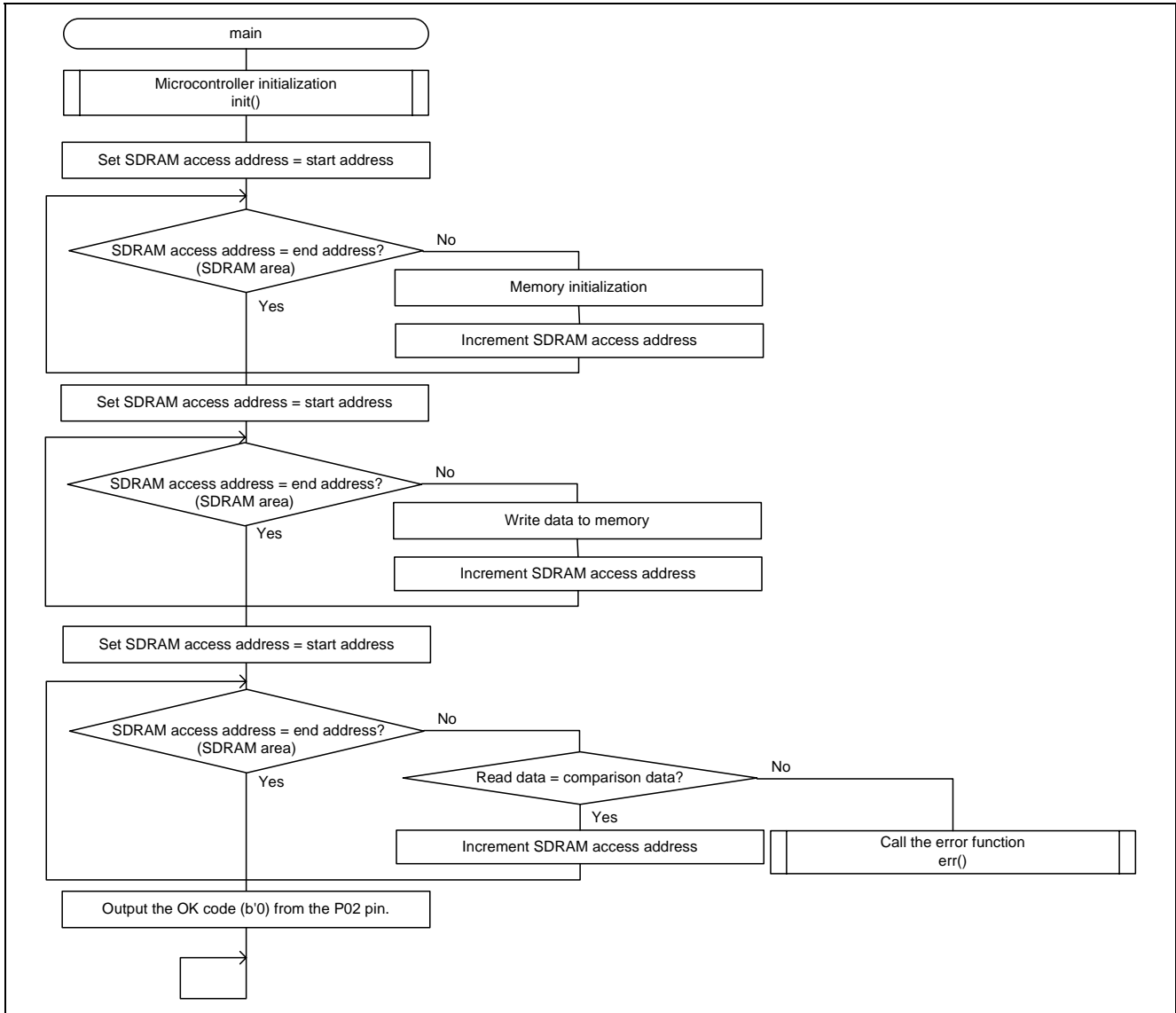


Figure 8 main() Function Flowchart

5.5.3 init() Function

(1) Functional description

The init() function initializes the functions used by the microcontroller.

(2) Arguments

None

(3) Return Values

None

(4) Flowchart

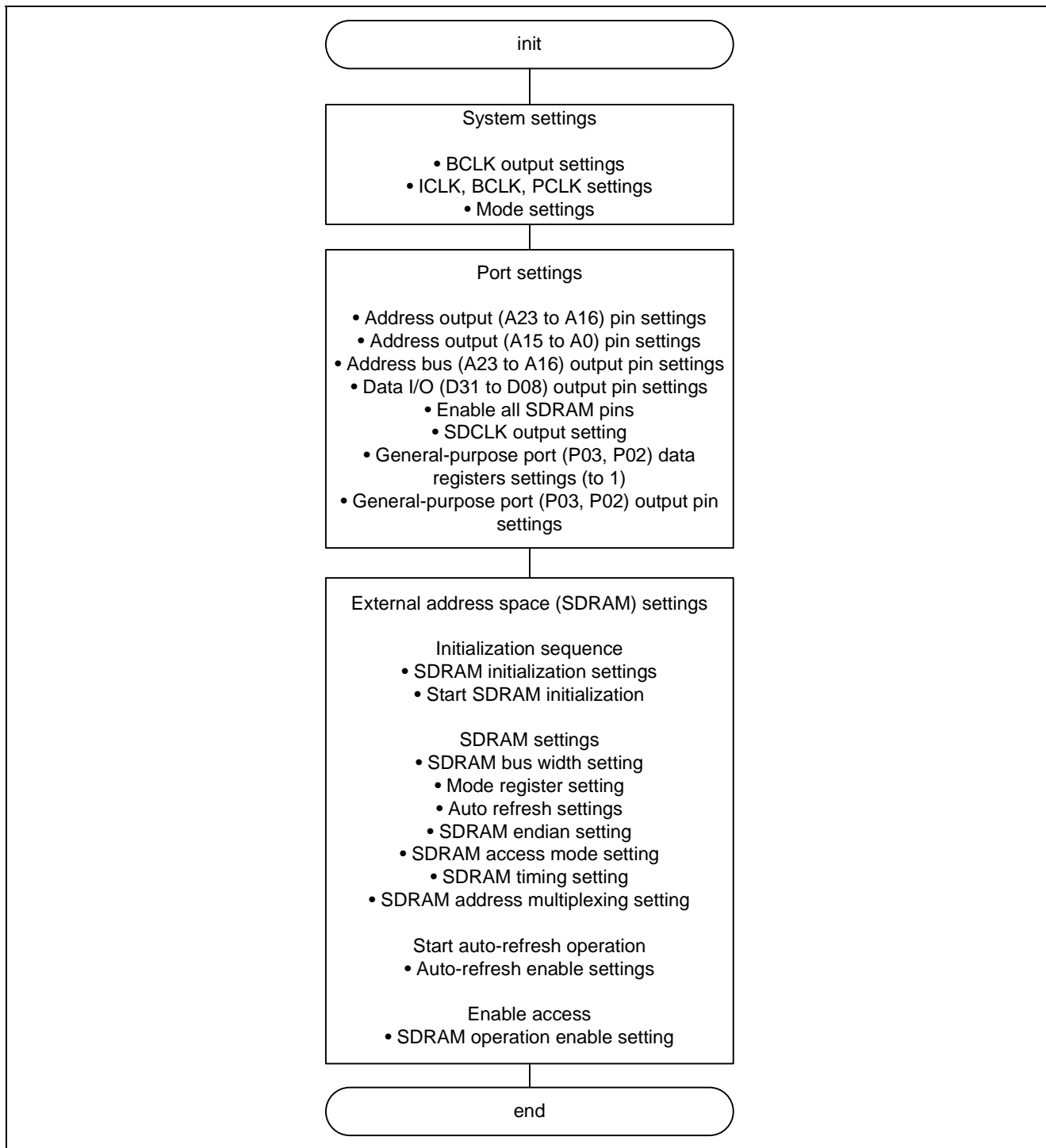


Figure 9 init() Function Flowchart

### 5.5.4 err() Function

#### (1) Functional description

The err() function outputs the error code for data compare match failure.

#### (2) Arguments

None

#### (3) Return Values

None

#### (4) Flowchart

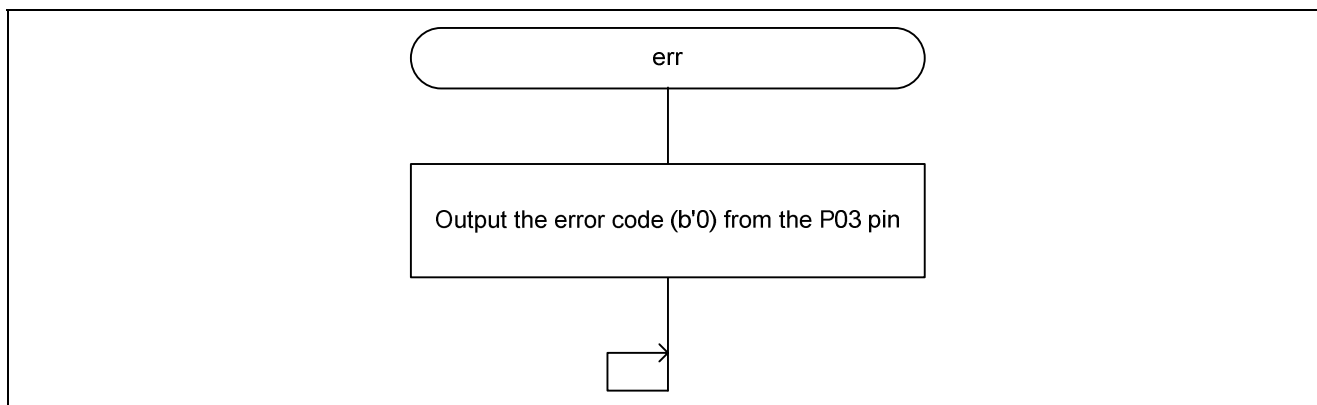


Figure 10 err() Function Flowchart

## 6. Reference Documents

- Hardware Manual  
RX62N Group, RX621 Group Hardware Manual  
(The latest version can be downloaded from the Renesas Electronics Web site.)
- Development Environment Manual  
RX Family C/C++ Compiler Package User's Manual  
(The latest version can be downloaded from the Renesas Electronics Web site.)
- Technical Update  
(The latest version can be downloaded from the Renesas Electronics Web site.)

## Website and Support

Renesas Electronics Website

<http://www.renesas.com/>

Inquiries

<http://www.renesas.com/inquiry>

All trademarks and registered trademarks are the property of their respective owners.



## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable.

When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

## Notice

- All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
- Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
- You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
- Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
- When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
- Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
- Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.  
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.  
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.  
"Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
- You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
- Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
- Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
- This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
- Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.  
(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.  
(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.



### SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

#### Renesas Electronics America Inc.

2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.  
Tel: +1-408-588-6000, Fax: +1-408-588-6130

#### Renesas Electronics Canada Limited

1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada  
Tel: +1-905-898-5441, Fax: +1-905-898-3220

#### Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K  
Tel: +44-1628-585-100, Fax: +44-1628-585-900

#### Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-65030, Fax: +49-211-6503-1327

#### Renesas Electronics (China) Co., Ltd.

7th Floor, Quantum Plaza, No.27 ZhichunLu Haidian District, Beijing 100083, P.R.China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

#### Renesas Electronics (Shanghai) Co., Ltd.

Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China  
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

#### Renesas Electronics Hong Kong Limited

Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

#### Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei, Taiwan  
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

#### Renesas Electronics Singapore Pte. Ltd.

1 HarbourFront Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: +65-6213-0200, Fax: +65-6278-8001

#### Renesas Electronics Malaysia Sdn.Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

#### Renesas Electronics Korea Co., Ltd.

11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea  
Tel: +82-2-558-3737, Fax: +82-2-558-5141