

RENESAS TECHNICAL UPDATE

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Title	Note on the R8C/Mx Series	Information Category	Technical Notification		
Applicable Product	R8C/Mx Series	Lot No.	---	Reference Document	

Note the following for the R8C/Mx Series.

1. Note on flash memory CPU rewrite mode (EW1 mode)

(1) Note

When setting the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled) and the FMR02 bit to 1 (EW1 mode) to execute CPU rewrite mode, it may not be executed correctly.

(2) Countermeasure

Execute the software command in the procedure shown in Figures 1 and 2 as a countermeasure. Figure 1 shows the procedure when suspend is disabled. Figure 2 shows the procedure when suspend is enabled.

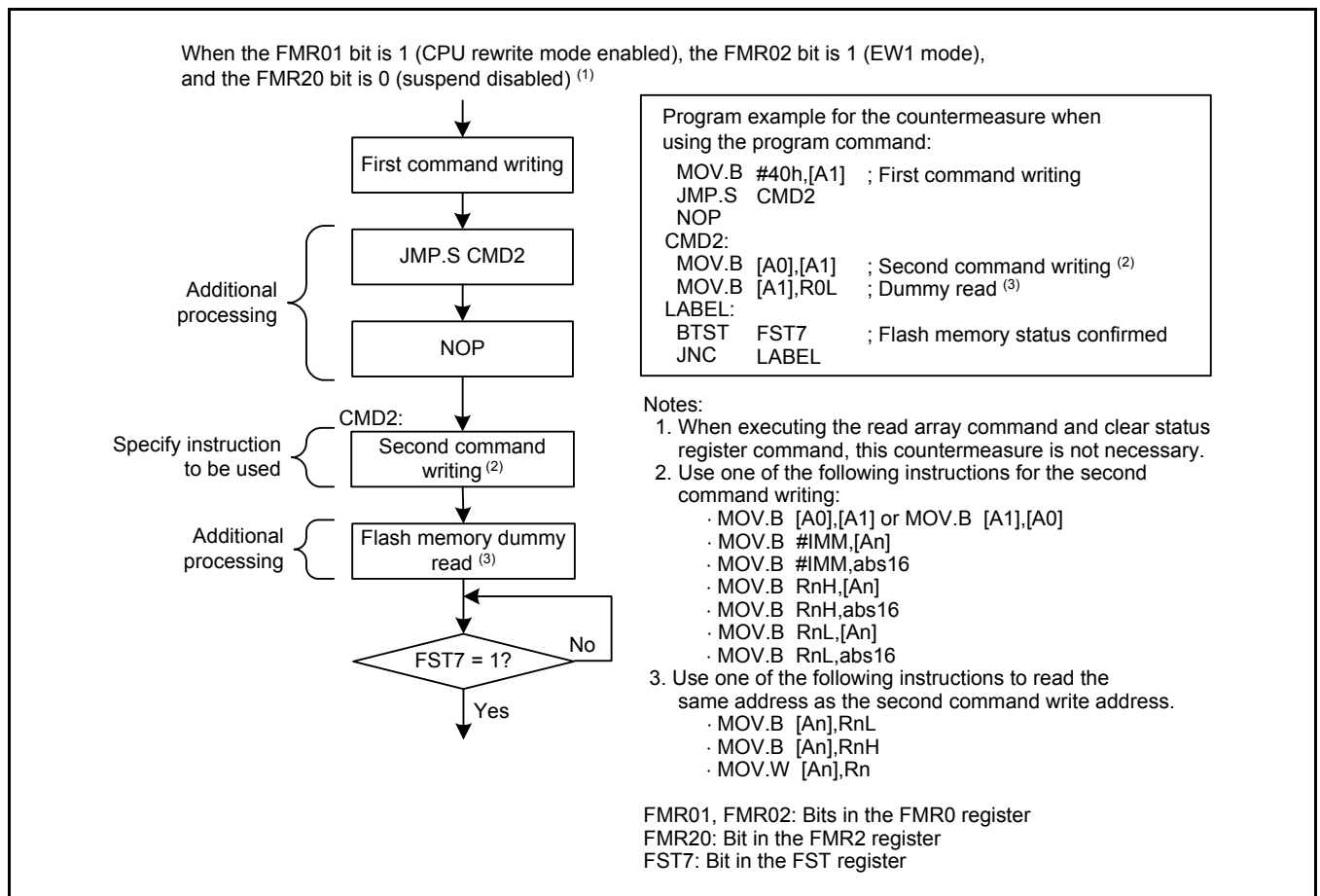
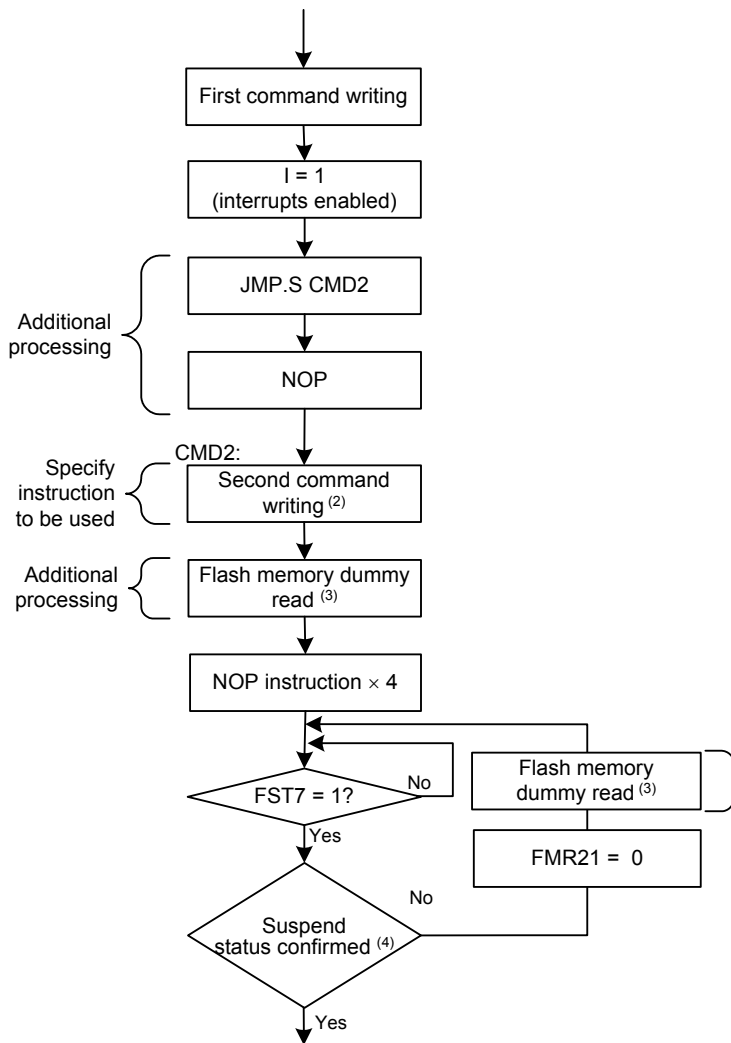


Figure 1 Procedure for Software Command Execution When Suspend is Disabled

When the FMR01 bit is 1 (CPU rewrite mode enabled), the FMR02 bit is 1 (EW1 mode), and the FMR20 bit is 1 (suspend enabled) ⁽¹⁾



Program example for the countermeasure when using the program command:

```

MOV.B #40h,[A1] ; First command writing
FSET I ; Interrupts enabled
JMP.S CMD2
NOP
CMD2:
MOV.B [A0],[A1] ; Second command writing (2)
MOV.B [A1],R0L ; Dummy read (3)
NOP
NOP
NOP
NOP
LABEL1:
BTST FST7 ; Flash memory status confirmed
JNC LABEL1
BTST FST3 ; Suspend status confirmed (4)
JNC LABEL2
BCLR FMR21
MOV.B [A1],R0L ; Dummy read (3)
JMP LABEL1
LABEL2:
    
```

Notes:

- When executing the read array command and clear status register command, this countermeasure is not necessary.
- Use one of the following instructions for the second command writing:
 - MOV.B [A0],[A1] or MOV.B [A1],[A0]
 - MOV.B #IMM,[An]
 - MOV.B #IMM,abs16
 - MOV.B RnH,[An]
 - MOV.B RnH,abs16
 - MOV.B RnL,[An]
 - MOV.B RnL,abs16
- Use one of the following instructions to read the same address as the second command write address.
 - MOV.B [An],RnL
 - MOV.B [An],RnH
 - MOV.W [An],Rn
- Confirm the suspend status using the FST3 bit for the program command, and the FST6 bit for the block erase command.

1: Flag in the CPU register
 FMR01, FMR02: Bits in the FMR0 register
 FMR20: Bit in the FMR2 register
 FST3, FST6, FST7: Bits in the FST register

Figure 2 Procedure for Software Command Execution When Suspend is Enabled

2. Note on low-consumption-current read mode

Please note when using low-consumption-current read mode by the FMR27 bit (low-current-consumption read mode enable bit) in the FMR2 register.

(1) Note when manipulating the FMR27 bit

Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-consumption-current read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-consumption-current read mode enabled).

Program example to enter stop mode:

```

BCLR    1,FMR0      ; CPU rewrite mode disabled
BCLR    7,FMR2      ; Low-consumption-current read mode disabled
BSET    0,PRCR      ; Writing to the CKSTPR register enabled
FSET    I           ; Interrupt enabled
BSET    0,CKSTPR    ; Stop mode
JMP.B   LABEL_001
LABEL_001:
NOP
NOP
NOP
NOP

```

Program example to enter wait mode:

When executing the WAIT instruction

```

BCLR    1,FMR0      ; CPU rewrite mode disabled
BCLR    7,FMR2      ; Low-consumption-current read mode disabled
FSET    I           ; Interrupt enabled
WAIT                    ; Wait mode
NOP
NOP
NOP
NOP

```

When setting the WAITM bit to 1

```

BCLR    1,FMR0      ; CPU rewrite mode disabled
BCLR    7,FMR2      ; Low-consumption-current read mode disabled
BSET    0,PRCR      ; Writing to the SCKCR register enabled
FCLR    I           ; Interrupt disabled
BSET    5, SCKCR    ; Wait mode
NOP
NOP
NOP
NOP
BCLR    0,PRCR      ; Writing to the SCKCR register disabled
FSET    I           ; Interrupt enabled

```

(2) Note on the FMSTP bit

Do not set the FMR27 bit to 1 while the FMSTP bit (flash memory stop bit) in the FMR0 register is 1 (flash memory stops).

3. Procedure for Reducing Power Consumption Using the FMSTP Bit

A procedure for reducing power consumption using the FMSTP bit in the hardware user's manual is shown as follows.

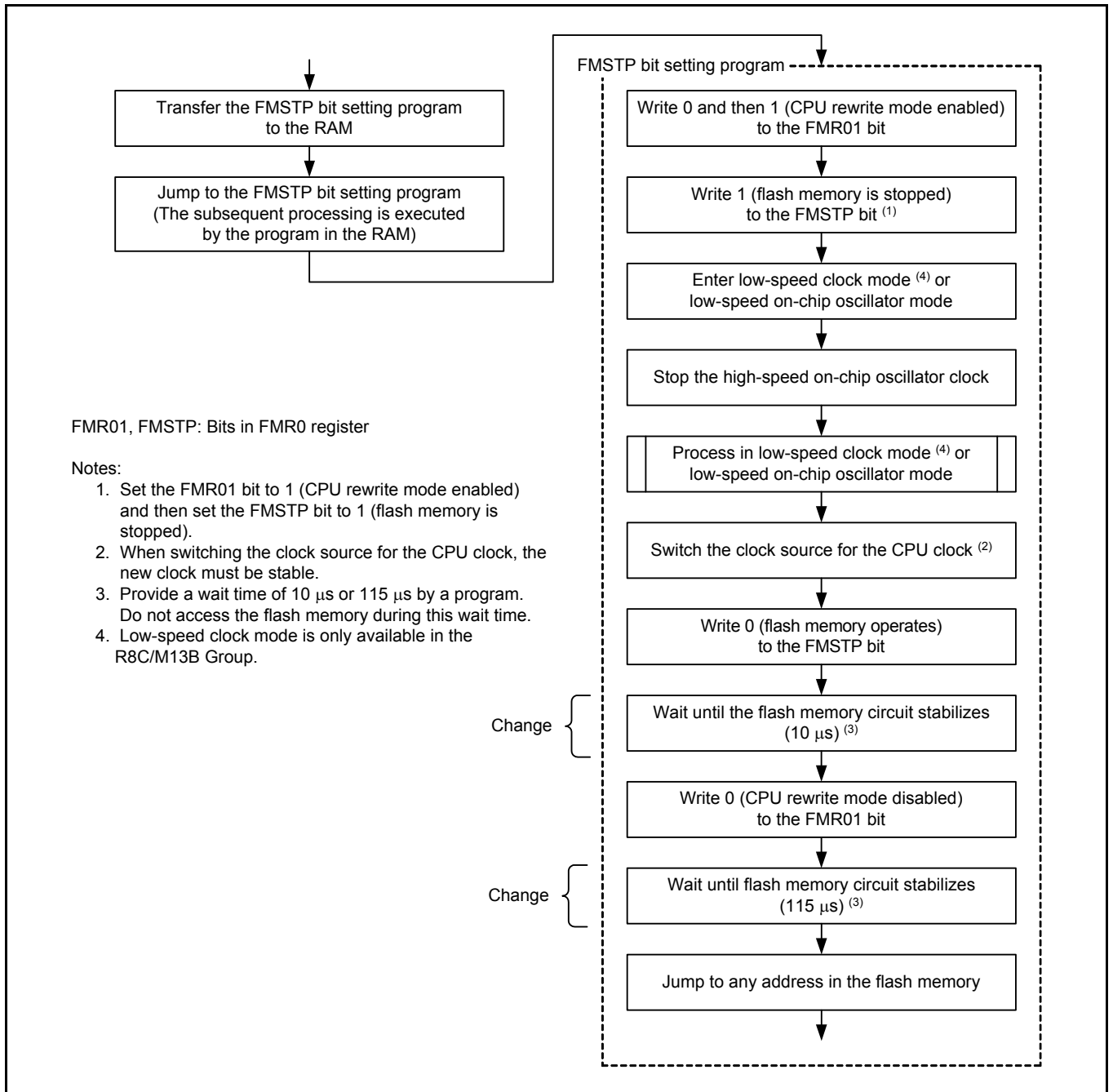


Figure 3. Procedure for Reducing Power Consumption Using the FMSTP Bit