

RX600 Series

R20AN0085EJ0101

Rev.1.01

M3S-FFT-LIB: FFT Library Introduction Guide

Jun 13, 2011

Introduction

This document explains M3S-FFT-LIB for the RX Family V.1.00 Release00E (hereafter referred to as "FFT library"). FFT library will differ depending on the MCUs. Fast Fourier Transform (FFT) is the fast algorithm for efficient implementation of the discrete Fourier transform (DFT). As is well known, the development of FFT by Cooley and Tukey in 1965 has led to phenomenal growth in its applications in digital signal processing.

The FFT library for the Renesas Microcomputer is written in optimized assembler.

Please refer to the User's Manual to understand how to use the software library. User's Manual is in M3S-FFT-LIB installer package.

Target Device

RX600 Series

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There are corrections in "7. FFT Library performance" of this document.

1. Structure of M3S-FFT-LIB

1. M3S-FFT-LIB for the RX Family V.1.00 Release01E
2. M3S-FFT-LIB for the RX Family V.1.00 Release01E Introduction Guide (r20an0085ej0101_rx_fft.pdf)
part number of this product : R0MRX60LF0010RRC

Table 1 FFT library product files

name	Description
Installer (setup.exe)	For Windows installer. Installer will show the FFT library agreement. If user admits this agreement, installer will copy the FFT library files to the path below. C:\Renesas\an_r20an0085ej_rx_fft_v100r01
FFT Library(lib)	
fft_rx_big_rtune.lib	FFT library for RX Family assembler tuning ver. (big endian) Library version 1.00
fft_rx_little_rtune.lib	FFT library for RX Family assembler tuning ver. (little endian) Library version 1.00
r_fft.h	FFT library header file
Sample program(sample)	
rx_fft	HEW Project file
Document(doc)	
r20uw0071ej0101_fft.pdf	User's Manual
r20an0085ej0101_rx_fft.pdf	Introduction Guide (this document)

2. Corresponding MCU

This product corresponds to RX family.

FFT library is built with the following compile option.

- compile option (little endian)

-cpu=rx600 -output=obj="\$(CONFIGDIR)\\$(FILELEAF).obj" -nologo

- compile option (big endian)

-cpu=rx600 -output=obj="\$(CONFIGDIR)\\$(FILELEAF).obj" -nologo -endian=big

3. Development environment

-Host OS

Windows XP • Windows NT 4.0 • Windows 2000 • Windows Me • Windows 98 • Windows 95

-Renesas Tool Requirements

Please ensure that when developing with this product, you have the same or newer versions than those listed below.

[Software]

-Integrated Development Environment

High Performance Embedded Workshop Version 4.08.00.011

-C compiler

C/C++ compiler package for RX family V.1.00 Release 00

-Debugger

RX Family Simulator/Debugger V.1.01.00.000

4. FFT Library ROM / RAM / stack size

FFT library for RX Family supports FFT points below.

Complex number FFT: 16, 32, 64 points

Real number FFT: 128, 256, 512, 1024 points

[ROM/RAM size]

FFT library for the RX Family assembler tuning ver (big endian)

ROM : 21604 byte

RAM : 0 byte

API	Stack size
R_cfft16	36
R_cfft32	36
R_cfft64	36
R_rfft128	16
R_rfft256	16
R_rfft512	16
R_rfft1024	16

FFT library for the RX Family assembler tuning ver (little endian)

ROM : 21671 byte

RAM : 0 byte

API	Stack size
R_cfft16	36
R_cfft32	36
R_cfft64	36
R_rfft128	16
R_rfft256	16
R_rfft512	16
R_rfft1024	16

5. FFT library section information

Section name	Type	Description
PFFT	program area	library program data
CFFT_2	constant data area	constant data: needs 2 byte alignment
CFFT_8	constant data area	constant data: needs 8 byte alignment

6. FFT library Version information

User can access FFT Library information with the variables listed below.

```
extern const char _aes_version[];
```

```
extern const char r_fft_a_version[];
```

BIG Endian: "M3S-FFT-LIB version 1.00 for RX BIG endian(ASSEMBLER TUNED).(Jun 13 2011, 13:38:38)"

Little Endian: "M3S-FFT-LIB version 1.00 for RX LITTLE endian(ASSEMBLER TUNED).(Jun 13 2011, 13:38:42)"

7. FFT Library performance

This section shows FFT Library performance below. The processing speed values are two types. The one is cycle, another one is time that RX600 series is set at 100MHz system clock.

API	processing speed	
	cycle [cycles]	time [usec]
R_cfft16	994	9.940
R_cfft32	3597	35.97
R_cfft64	6928	69.28
R_rfft128	4029 12695	40.29 126.95
R_rfft256	8094 28826	80.94 288.26
R_rfft512	16224 63588	162.24 635.88
R_rfft1024	32733 141038	327.33 1410.38

8. Library version information

ver	change
1.00	first release

Website and Support

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<http://www.renesas.com/>

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jun.06.13	—	First edition issued
1.01	Jun.06.13	—	Fixed User's Manual Added real FFT sample program

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable.

When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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