

Thank you for purchasing the flash memory programmer PG-FP5.

This document describes specifications that have been added or changed, restrictions, and cautions on using the PG-FP5. Also see the user's manual of the PG-FP5 for cautions on using the PG-FP5.

See the following documents for restrictions related to the target device.

- User's manual of target device
- Restriction notification document for target device

Chapter 1 Product Version	2
Chapter 2 Additions and Changes to Specifications	3
Chapter 3 Restrictions	10

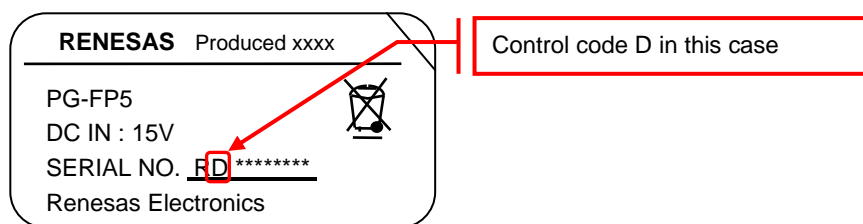
Chapter 1 Product Version

Item No.	Control Code ^{Note 1}	Firmware	FPGA	Programming GUI	Remark
<1>	A	V1.00	V1	V1.00	
<2>		V1.01	V1	V1.00	
<3>		V2.00	V2	V2.00	
<4>		V2.01	V2	V2.01	
<5>		V2.02	V2	V2.02	
<6>	A, C ^{Note 2}	V2.03	V2	V2.03	
<7>		V2.04	V2	V2.03	
<8>		V2.05	V2	V2.05	
<9>	A, C, D ^{Note 2}	V2.06	V4	V2.06	
<10>		V2.07	V4	V2.07	

To check the version, perform the following procedure:

- Firmware: On the menu bar, click **Programmer**, and then select **Reset**.
- FPGA: On the menu bar, click **Programmer**, and then select **Reset**.
- Programming GUI: On the menu bar, click **Help**, and then select **About FP5....**

Notes 1. The control code is the second digit from the left in the 10-digit serial number. If the product has been upgraded, a label indicating the new version is attached to the product and the x in **V-UP x** on this label indicates the control code.



- 2.** Products with control code A, C, and D are functionally equivalent. These products can be used in combination with the relevant version of the firmware, FPGA, and programming GUI.

Chapter 2 Additions and Changes to Specifications

2.1 List of additions and changes to specifications

No.	Additions and Changes to Specifications	Product Version (Item No.)									
		<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>
1	Modification of Cancel button specification	x	○	○	○	○	○	○	○	○	○
2	Addition of FP5 Manager functions	x	x	○	○	○	○	○	○	○	○
3	Addition of communication command functions	x	x	○	○	○	○	○	○	○	○
4	Addition of remote connector functions	x	x	○	○	○	○	○	○	○	○
5	Change of location of Erase memory before download check box	x	x	○	○	○	○	○	○	○	○
6	Addition of specification related to Checksum command display	x	x	○	○	○	○	○	○	○	○
7	Addition of program file size check function	x	x	○	○	○	○	○	○	○	○
8	Addition of [Enable target RESET] function	x	x	○	○	○	○	○	○	○	○
9	Change of specification related to action log window view	x	x	○	○	○	○	○	○	○	○
10	Change of specification related to message display view	x	x	○	○	○	○	○	○	○	○
11	Addition of specification that enables specification of storage destination for ESF and PR5 files	x	x	○	○	○	○	○	○	○	○
12	Addition of program file upload function	x	x	○	○	○	○	○	○	○	○
13	Change of GUI language to Japanese for Japanese version OS <Japanese version only>	x	x	x	○	○	○	○	○	○	○
14	Addition of specification of UART communication at 500 kbps	x	x	x	○	○	○	○	○	○	○
15	Addition of [Wide Voltage mode] function	x	x	x	x	○	○	○	○	○	○
16	Change of layout in Block protection area	x	x	x	x	○	○	○	○	○	○
17	Addition of HCUHEX file reading function	x	x	x	x	x	○	○	○	○	○
18	Addition of program file size monitoring function	x	x	x	x	x	○	○	○	○	○
19	Change of power button specification	x	x	x	x	x	○	○	○	○	○
20	Addition of [Disable FSW reprogramming] function	x	x	x	x	x	x	x	○	○	○
21	Addition of [OCD security ID setting] function and [Option bytes setting] function	x	x	x	x	x	x	x	○	○	○
22	Support of 14-pin interface	x	x	x	x	x	x	x	x	○	○
23	Support of RL78 family	x	x	x	x	x	x	x	x	○	○
24	Support of RX600 series	x	x	x	x	x	x	x	x	○	○
25	Change of Windows supported	x	x	x	x	x	x	x	x	○	○
26	Writing to 78K0 microcontrollers by using an external UART clock	x	x	x	x	x	x	x	x	○	○
27	Change of installer	x	x	x	x	x	x	x	x	○	○
28	Addition of device image file load function	x	x	x	x	x	x	x	x	○	○
29	Support of R8C family	x	x	x	x	x	x	x	x	x	○
30	Support of SuperH family	x	x	x	x	x	x	x	x	x	○

–: Not relevant, x: Specification change not implemented, ○: Specification change implemented

2.2 Details of additions and changes to specifications

No. 1 Modification of **Cancel** button specification

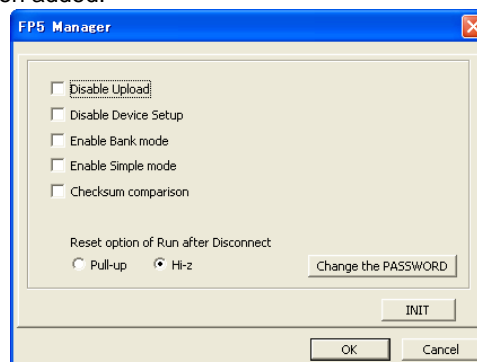
Description: The function of the **Cancel** button on the PG-FP5 main unit has been modified so that cancellation, which was applied to all commands, is only applied to the **Read** command.

Implementation: This item has been implemented in products with control code A (firmware: V1.01, FPGA: V1, GUI: V1.00).

No. 2 Addition of FP5 Manager functions

Description: The following FP5 Manager functions have been added.

- Password function
- Upload disable function
- Device setup disable function
- Bank mode enable function
- Simple mode enable function
- Checksum compare function
- Reset pin characteristics switch function



Implementation: This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 3 Addition of communication command functions

Description: The PG-FP5 main unit can now be manipulated via communication software by using communication commands, with the PG-FP5 connected to the host machine via the serial connector.

Implementation: This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 4 Addition of remote connector functions

Description: The PG-FP5 main unit can now be manipulated from remote locations by connecting an external control unit to the PG-FP5 via the remote connector. Remote operation enables manipulating and checking of programming and PASS/ERROR display from the external control unit.

Implementation: This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 5 Change of location of Erase memory before download check box

Description: The location of the **Erase memory before download** check box has been moved from the **Download file** dialog box to the **Object HEX file** area on the **Target** tab in the **Setup** dialog box.

Implementation: This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 6 Addition of specification related to Checksum command display

Description: The checksum result is now displayed in the message display even while the **Checksum** command is being executed, either via the programming GUI or the command option during standalone operation.

Implementation: This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 7 Addition of program file size check function

Description: If the addresses of a downloaded program file are out of the address range set in the **Operation mode** area on the **Standard** tab in the **Setup** dialog box, the warning message `WARNING: HEX file exceeds target device flash range.` is now displayed in the action log window when the **Program**, **Verify**, or **Autoprocedure(E.P.)** command is executed.

Implementation: This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 8 Addition of [Enable target RESET] function

Description: The [Enable target RESET] function has been added. When this function is enabled, the RESET pin goes into input mode (Hi-Z), and the FP5 detects rising and falling edges input to the RESET pin immediately after executing a command.

Implementation: This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 9 Change of specification related to action log window view

Description: The message displayed in the action log window after command execution has been changed from OK to PASS. In addition, the error number is now displayed with the error message, as displayed in the message display.

Implementation: This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 10 [Change of specification related to message display view](#)

Description: In conjunction with the addition of new functions in control code A (firmware: V2.00, FPGA: V2, GUI: V2.00), the display of all commands has been updated.

Implementation: This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 11 [Addition of specification that enables specification of storage destination for ESF and PR5 files](#)

Description: In products with control code A (firmware: V1.01, FPGA: V1, GUI: V1.00) or earlier, the ESF and PR5 files can only be stored in the FP5_PRJ folder where the programming GUI is installed, but these files can now be stored in any folder.

Implementation: This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 12 [Addition of program file upload function](#)

Description: A function to upload program files has been added. Uploading can be disabled by using an FP5 Manager function.

Implementation: This item has been implemented in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 13 [Change of GUI language to Japanese for Japanese version OS <Japanese version only>](#)

Description: The GUI language has been changed to Japanese when used in a Japanese OS.

Implementation: This item has been implemented in products with control code A (firmware: V2.01, FPGA: V2, GUI: V2.01).

No. 14 [Addition of specification of UART communication at 500 kbps](#)

Description: The specifications have been changed so that 500 kbps can now be selected as the baud rate of UART communication, even if a target device other than a 78K0R microcontroller is selected. However, communication at 500 kbps is not available if this specification is not supported in the target device. For the baud rate supported in each target device, see the user's manual for the device or a supplementary document containing the parameter files. If a 78K0R microcontroller is used as the target device, communication at 500 kbps is available when using Programming GUI V1.00 and later.

Implementation: This item has been implemented in products with control code A (firmware: V2.01, FPGA: V2, GUI: V2.01).

No. 15 Addition of **Wide Voltage mode** function

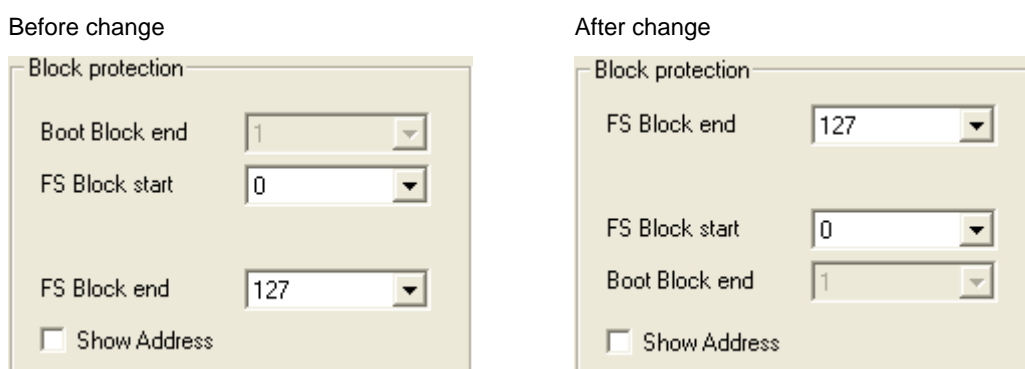
Description: The **Wide Voltage mode** check box has been added to the **Command options** area.

If this check box is selected, commands are executed in the wide voltage mode. If this check box is not selected, commands are executed in the full-speed mode. This check box is available when a device supporting this function is selected. For details about the wide voltage mode and full-speed mode, see the user's manual of each device.

Implementation: This item has been implemented in products with control code A (firmware: V2.02, FPGA: V2, GUI: V2.02).

No. 16 Change of layout in **Block protection** area

Description: The layout in the **Block protection** area has been changed.



Implementation: This item has been implemented in products with control code A (firmware: V2.02, FPGA: V2, GUI: V2.02).

No. 17 Addition of HCUHEX file reading function

Description: The HCUHEX files created using the HEX Consolidation Utility (HCU), which is used for generating ROM code for ordering Renesas Electronics preprogrammed flash memory devices, can now be read.

Implementation: This item has been implemented in products with control code A, C (firmware: V2.03, FPGA: V2, GUI: V2.03).

No. 18 Addition of program file size monitoring function

Description: The **Program file size monitor function** check box has been added to the **FP5 Manager** dialog box.

If this check box is selected, execution of the **Program** command is suspended if the program file is larger than the area to be written to.

Implementation: This item has been implemented in products with control code A, C (firmware: V2.03, FPGA: V2, GUI: V2.03).

No. 19 [Change of power button specification](#)

Description: The power of the PG-FP5 can now be turned on by pressing the POWER button for about 1 second.

Implementation: This item has been implemented in products with control code A, C (firmware: V2.03, FPGA: V2, GUI: V2.03).

No. 20 [Addition of \[Disable FSW reprogramming\] function](#)

Description: The [Disable FSW reprogramming] function has been added.

Implementation: This item has been implemented in products with control code A, C (firmware: V2.05, FPGA: V2, GUI: V2.05).

No. 21 [\[OCD security ID setting\] function and \[Option bytes setting\] function](#)

Description: The [OCD security ID setting] function and [Option bytes setting] function have been added.

Implementation: This item has been implemented in products with control code A, C (firmware: V2.05, FPGA: V2, GUI: V2.05).

No. 22 [Support of 14-pin interface](#)

Description: A target cable (14pin type) compatible with the 14-pin interface of the E1 emulator will be provided in addition to the existing target cable (16pin type), starting from July 2011.

Implementation: This item will be implemented in products with control code A, C, D (firmware: V2.06, FPGA: V4, GUI: V2.06).

No. 23 [Support of RL78 family](#)

Description: The RL78 family is now supported.

Implementation: This item has been implemented in products with control code A, C, D (firmware: V2.06, FPGA: V4, GUI: V2.06).

No. 24 [Support of RX600 series](#)

Description: The RX600 series is now supported.

Implementation: This item has been implemented in products with control code A, C, D (firmware: V2.06, FPGA: V4, GUI: V2.06).

No. 25 [Change of supported Windows Versions](#)

Description: The 32-bit and 64-bit editions of Windows 7 and the 64-bit edition of Windows Vista are now supported. Windows 2000 is no longer supported.

Implementation: This item has been implemented in products with control code A, C, D (firmware: V2.06, FPGA: V4, GUI: V2.06).

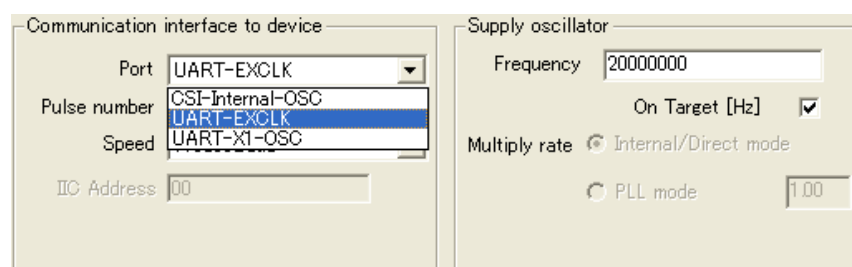
No. 26 Writing to 78K0 microcontrollers by using an external UART clock

Description: When writing to 78K0 microcontrollers by using UART communication, the PG-FP5 can now perform writing to a target system in which an external clock is input to the microcontroller's EXCLK pin. To enable this feature, select **UART-EXCLK** in the **Port** list box, select the **On Target** check box, and input the relevant frequency to the **Frequency** box.

Along with the addition of this feature, the options in the **Port** list box have been changed as follows:

UART-Ext-OSC → UART-X1-OSC (select when using an external resonator clock)

UART-Ext-QB2CLK → UART-EXCLK (select when using an external clock or the FP5 clock)



Implementation: This item has been implemented in products with control code A, C, D (firmware: V2.06, FPGA: V4, GUI: V2.06).

No. 27 Change of installer

Description: The installer has been changed to an installer for CubeSuite+.

Implementation: This item has been implemented in products with control code A, C, D (firmware: V2.06, FPGA: V4, GUI: V2.06).

No. 28 Addition of device image file load function

Description: A function to enable loading of device image files (DDI files) supported by the Flash Development Toolkit has been added. Note that this function does not include a file-save capability. Note also that DDI files cannot be read by a hexadecimal editor.

Implementation: This item has been implemented in products with control code A, C, D (firmware: V2.06, FPGA: V4, GUI: V2.06).

No. 29 Support of R8C family

Description: The R8C family is now supported.

Implementation: This item has been implemented in products with control code A, C, D (firmware: V2.07, FPGA: V4, GUI: V2.07).

No. 30 Support of SuperH family

Description: The SuperH family is now supported.

Implementation: This item has been implemented in products with control code A, C, D (firmware: V2.07, FPGA: V4, GUI: V2.07).

Chapter 3 Restrictions

3.1 Restriction List

No.	Restrictions	Product Version (Item No.)									
		<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>
1	Restriction whereby Invalid Device Port is displayed	x	x	○	○	○	○	○	○	○	○
2	Restriction whereby standalone operation can no longer be performed under specific conditions	x	○	○	○	○	○	○	○	○	○
3	Restriction whereby erase is performed even if Erase memory before download is not selected	x	x	○	○	○	○	○	○	○	○
4	Restriction whereby status bar is displayed incorrectly	x	x	○	○	○	○	○	○	○	○
5	Restriction whereby RESET pin is always pulled up to 5 V when Run after Disconnect is set	x	x	○	○	○	○	○	○	○	○
6	Restriction whereby no clock is supplied when FP5CLK is selected for pseudo 3-wire communication or I ² C communication	x	x	○	○	○	○	○	○	○	○
7	Restriction whereby Motorola S type program file is not displayed in the list box	x	x	○	○	○	○	○	○	○	○
8	Restriction whereby FLMD0 pin outputs low level when 78K0S (single-wire UART) is used	x	x	○	○	○	○	○	○	○	○
9	Restriction whereby lowercase letters are illegally converted to uppercase letters when upprm or upset command is executed	x	x	x	○	○	○	○	○	○	○
10	Restriction whereby an invalid checksum result is obtained if a program file is downloaded in Simple mode	-	-	x	○	○	○	○	○	○	○
11	Restriction whereby bank switching for the program file cannot be specified in bank mode	-	-	x	○	○	○	○	○	○	○
12	Restriction on reading a Motorola S1-record hex format program file	x	x	x	x	x	○	○	○	○	○
13	Restriction related to installation of USB driver	-	-	-	-	x	○	○	○	○	○
14	Restriction whereby the error NAND flash - Mapping Error is displayed	x	x	x	x	x	x	○	○	○	○
15	Restriction whereby the message display is not updated	x	x	x	x	x	x	x	○	○	○
16	Restriction which cannot get the flash options of RL78	x	x	x	x	x	x	x	○	○	○

-: Not relevant, x: Applicable, ○: Corrected

3.2 Restriction Details

No. 1 Restriction whereby Invalid Device Port is displayed

Description: When a PR5 file is downloaded, the message Invalid Device Port might be displayed in the action log window. After that, PR5 files can no longer be downloaded correctly.

Workaround: There is no workaround.

Action: This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 2 Restriction whereby standalone operation can no longer be performed under specific conditions

Description: If command execution is continued by using control buttons on the PG-FP5 main unit while the Programming GUI is not running, the message `ERROR: 800 Res. by Watchdog` is displayed in the message display on the PG-FP5 main unit and the subsequent operations might no longer be able to be performed.

Workaround: There is no workaround. When this situation occurs, control of the **POWER** button is also unavailable. Therefore, disconnect the AC adapter and connect it again to restart the PG-FP5.

Action: This issue has been corrected in products with control code A (firmware: V1.01, FPGA: V1, GUI: V1.00).

No. 3 Restriction whereby erase is performed even if Erase memory before download is not selected

Description: Erase is performed even if the **Erase memory before download** check box is not selected in the **Download file** dialog box, which is opened via the **Object HEX file** area on the **Target** tab in the **Setup** dialog box.

Workaround: There is no workaround.

Action: This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 4 Restriction whereby status bar is displayed incorrectly

Description: The status bar is displayed incorrectly in the following cases:

- (1) An error is displayed erroneously if it takes five or more seconds for SUM data to be returned during **Checksum** command execution.
- (2) PASS is displayed erroneously if the code flash is verified to be OK but the data flash is reported as having an error.

Workaround: There is no workaround.

Action: This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 5 Restriction whereby RESET pin is always pulled up to 5 V when Run after Disconnect is set

Description: The RESET pin of the PG-FP5 must go into the Hi-Z state when **Run after Disconnect** is set, but it is pulled up to 5 V.

Workaround: There is no workaround.

Action: This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 6 Restriction whereby no clock is supplied when FP5CLK is selected for pseudo 3-wire communication or I²C communication

Description: No clock is supplied when **FP5CLK** is selected for pseudo 3-wire communication or I²C communication.

Workaround: There is no workaround.

Action: This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 7 Restriction whereby Motorola S type program file is not displayed in the list box

Description: When a program file of Motorola S type (except for *.hex and *.rec) is selected in the **Download file** dialog box which is opened via the **Object HEX file** area on the **Target** tab in the **Setup** dialog box, the file is not displayed in the list box in the **Object HEX file** area.

Workaround: There is no workaround.

Action: This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 8 Restriction whereby FLMD0 pin outputs low level when 78K0S (single-wire UART) is used

Description: If the CLK and FLMD0 pins are shorted in the target system when 78K0S (single-wire UART) is used, the FLMD0 pin that should output Hi-Z incorrectly outputs a low level, which disturbs programming. (This restriction is applicable only when a microcontroller that uses the FLMD0 pin was used before using 78K0S (single-wire UART).)

Workaround: Execute the **Reset** command of the PG-FP5 or turn off and then on the PG-FP5 power before using 78K0S (single-wire UART); the FLMD0 pin afterward outputs Hi-Z.

Action: This issue has been corrected in products with control code A (firmware: V2.00, FPGA: V2, GUI: V2.00).

No. 9 [Restriction whereby lowercase letters are illegally converted to uppercase letters when `upprm` or `upset` command is executed](#)

Description: The letter “a” in the format version is illegally converted to “A” when the `upprm` command is executed. The extensions of parameter files are illegally converted to uppercase letters when the `upset` command is executed. Use of the files created by these commands does not cause any problems.

Workaround: There is no workaround.

Action: This issue has been corrected in products with control code A (firmware: V2.01, FPGA: V2, GUI: V2.01).

No. 10 [Restriction whereby an invalid checksum result is obtained if a program file is downloaded in Simple mode](#)

Description: If a program file that includes data flash is downloaded in Simple mode, the checksum result to be displayed in the message display on the PG-FP5 main unit, which should indicate the checksum of the code flash and data flash areas, indicates the checksum of the code flash area only.

Workaround: There is no workaround.

Action: This issue has been corrected in products with control code A (firmware: V2.01, FPGA: V2, GUI: V2.01).

No. 11 [Restriction whereby bank switching for the program file cannot be specified in bank mode](#)

Description: When the PG-FP5 runs in bank mode and if a programming area is selected via a bank signal from the remote connector, the programming area selected via the bank signal should usually be selected, but the program file in the programming area selected by the Programming GUI is selected. The settings selected via the bank signal are then applied to PR5 and ESF files.

Example: Programming area number selected by Programming GUI: 0

Programming area number selected via bank signal: 1

In this case, PR5 and ESF files in programming area 1 and the program file in programming area 0 are specified.

Workaround: There is no workaround.

Action: This issue has been corrected in products with control code A (firmware: V2.01, FPGA: V2, GUI: V2.01).

No. 12 [Restriction on reading a Motorola S1-record hex format program file](#)

Description: If a program file in the Motorola S1-record hex format is read to the FP5, program files saved in the specified programming area become invalid.

Workaround: There is no workaround.

Action: This issue has been corrected in products with control code A or C (firmware: V2.03, FPGA: V2, GUI: V2.03).

No. 13 Restriction related to installation of USB driver

Description: If a PG-FP5 unit is connected to a USB port to which another FP5 unit with a different serial number was connected on the same host, the USB driver is not automatically recognized and installation of the USB driver is requested.

Workaround: There is no workaround.

Action: This issue has been corrected in products with control code A or C (firmware: V2.03, FPGA: V2, GUI: V2.03).

No. 14 Restriction whereby the error NAND flash - Mapping Error is displayed

Description: If the PG-FP5 is used continuously while conditions (1) and (2) below are satisfied, the error below might be displayed in the action log window when a program file is downloaded or a writing command is executed.

(1) A program file that has a cluster of FFh data that is 16 KB or longer is used.

(2) The program file described in (1) is frequently downloaded.

Displayed error:

```
*** System Error(s), Warning(s):  
Warning: NAND flash - Mapping Error
```

Even if the above error is displayed, downloading the program or executing the **Program** command is performed correctly.

Workaround: There is no workaround.

Action: This issue has been corrected in products with control code A or C (firmware: V2.04, FPGA: V2, GUI: V2.03).

No. 15 Restriction whereby the message display is not updated

Description: The writing status shown in the message display on the PG-FP5 unit might freeze and no longer be updated. (Even if this problem occurs, a command that downloads or writes a program runs normally.)

Workaround: There is no workaround.

Action: This issue has been corrected in products with control code A or C (firmware: V2.04, FPGA: V2, GUI: V2.03).

No. 16 Restriction which cannot get the flash options of RL78

Description: If the PG-FP5 executes **Get Flash options** command to RL78 valid of security setting, `E1601 Protect error.` is displayed, the PG-FP5 cannot get the flash options.

Action: This issue has been corrected in products with control code A, C or D (firmware: V2.07, FPGA: V4, GUI: V2.07).

All trademarks and registered trademarks are the property of their respective owners.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
"Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.
(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.
(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.



SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com>" for the latest and detailed information.

Renesas Electronics America Inc.

2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited

1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.

7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.

Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited

Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852-2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.

1 harbourFront Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.

11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141