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## Chapter 1. Target Devices

Below is a list of devices supported by the V850ES/Sx2 simulator.

Nickname	Device name
V850ES/SG1	μPD703249Y,μPD703252Y,μPD703253Y
V850ES/SG2	μPD703260Y,μPD703261Y,μPD703262Y,μPD703263Y,μPD703270Y,μPD703271Y, μPD703272Y,μPD703273Y,μPD703280Y,μPD703281Y,μPD703282Y,μPD703283Y, μPD70F3261Y,μPD70F3263Y,μPD70F3271Y,μPD70F3273Y,μPD70F3281Y, μPD70F3283Y
V850ES/SJ2	μPD703264Y,μPD703265Y,μPD703266Y,μPD703274Y,μPD703275Y,μPD703276Y, μPD703284Y,μPD703285Y,μPD703286Y,μPD703287Y,μPD703288Y,μPD70F3264Y, μPD70F3266Y,μPD70F3274Y,μPD70F3276Y,μPD70F3284Y,μPD70F3286Y, μPD70F3288Y
V850ES/SG2-H	μPD703262HY,μPD703263HY,μPD703272HY,μPD703273HY,μPD703282HY, μPD703283HY,μPD70F3263HY,μPD70F3273HY,μPD70F3283HY
V850ES/SJ2-H	μPD703265HY,μPD703266HY,μPD703275HY,μPD703276HY,μPD703285HY, μPD703286HY,μPD703287HY,μPD703288HY,μPD70F3266HY,μPD70F3276HY, μPD70F3286HY,μPD70F3288HY
V850ES/SG3	μPD70F3333,μPD70F3334,μPD70F3335,μPD70F3336,μPD70F3340,μPD70F3341, μPD70F3342,μPD70F3343,μPD70F3350,μPD70F3351,μPD70F3352,μPD70F3353
V850ES/SJ3	μPD70F3344,μPD70F3345,μPD70F3346,μPD70F3347,μPD70F3348,μPD70F3354, μPD70F3355,μPD70F3356,μPD70F3357,μPD70F3358,μPD70F3364,μPD70F3365, μPD70F3366,μPD70F3367,μPD70F3368
V850E/SJ3-H	μPD70F3474,μPD70F3475,μPD70F3476,μPD70F3477,μPD70F3478,μPD70F3479, μPD70F3931,μPD70F3932,μPD70F3933,μPD70F3934,μPD70F3935,μPD70F3936, μPD70F3937,μPD70F3938,μPD70F3939
V850E/SK3-H	μPD70F3480,μPD70F3481,μPD70F3482,μPD70F3486,μPD70F3487,μPD70F3488, μPD70F3925,μPD70F3926,μPD70F3927

## Chapter 2. User's Manuals

Please read the following user's manuals together with this document.

Manual Name	Document Number
CubeSuite+ V1.01.00 V850 Debug	R20UT0734EJ0100
CubeSuite+ V1.01.00 Message	R20UT0736EJ0100

## Chapter 3. Key Word for Uninstallation

To uninstall this product, use the integrated uninstaller (uninstalls CubeSuite+).

## Chapter 4. Changes

This chapter describes changes from V3.00.00 to V3.00.01.

### 4.1 Specifications changed

#### 4.1.1 Simulation on CubeSuite+ V1.01.00

Support simulation on CubeSuite+ V1.01.00. There is no functional change.

## Chapter 5. Cautions

This section describes cautions for using the V850ES/Sx2 simulator. The following two types of caution are described:

- Differences between target devices and simulator : Differences from behavior of target devices due to simulator specifications
- Notes for using simulator GUI : Notes for using the simulator GUI window

### 5.1 Differences between target devices and simulator

#### 5.1.1 Unsupported peripheral functions

The simulator does not support the following peripheral functions of the target device (the following functions cannot be debugged on the simulator).

- \* Flash self programming function
- \* CRC function
- \* ROM correction function
- \* CAN controller
- \* IEBus controller
- \* Clock monitor
- \* Regulator
- \* IIC

#### 5.1.2 Reset

If a reset is generated by the low voltage detector circuit, the simulator will display "STANDBY" in the status bar. (The status is actually reset, not standby.)

And the behavior differs as follows if a reset is generated by the RESET pin.

[Target device]

Goes into reset status when the RESET pin goes to low level. Reset status is released when it goes to high level.

[Simulator]

Does not go into reset status when the RESET pin goes to low level. When it goes to high level, the simulator momentarily goes into reset status, and then the reset status is released immediately.

### 5.1.3 Oscillation stabilization time and lock-up time of clock generator

The simulator does not simulate the oscillation stabilization time of the clock generator. For this reason, no matter what value the oscillation stabilization time selection register (OSTS) is set to, the simulator's oscillation stabilization time is always 0 seconds. Therefore, the value of CCLS register is always "00H". The simulator also does not simulate the PLL's lock-up time. No matter what value the PLL lock-up time specification register (PLLS) is set to, the lock-up time is always 0 seconds. Additionally, bit 0 (the LOCK bit) of the lock register (LOCKR) is cleared at the same time as the above lock-up.

### 5.1.4 Internal feedback resistor of main clock and sub clock

The simulator does not simulate the internal feedback resistor of the main clock or sub clock. For this reason, the main clock and sub clock will always oscillate, regardless of the settings of the MFRC and FRC bits on the processor clock control register (PCC).

### 5.1.5 Port function

If both of the conditions below are met, then the simulator will ignore writes to the port registers (e.g. P0 and PDL). Don't perform writes under the conditions below.

[Conditions for ignoring writes to port registers]

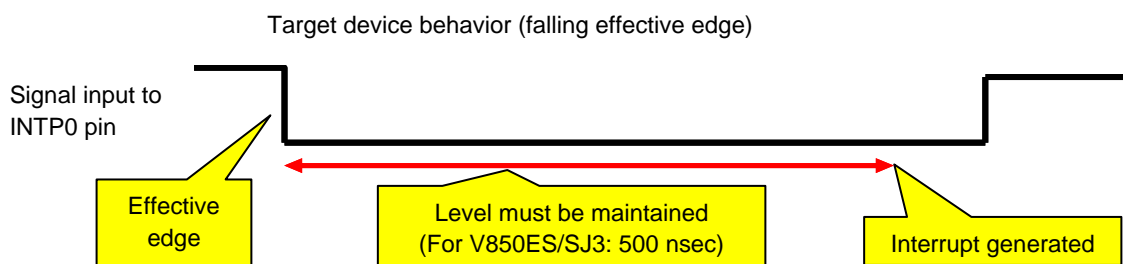
- \* The corresponding bit of the port mode control register (e.g. PMC0 or PMCDL) is set to 1 (port's dual function is enabled)
- \* The corresponding bit of the port mode register (e.g. PM0 or PMDL) is clear to 0 (set to output mode)

### 5.1.6 Noise reduction circuit for external-interrupt pin

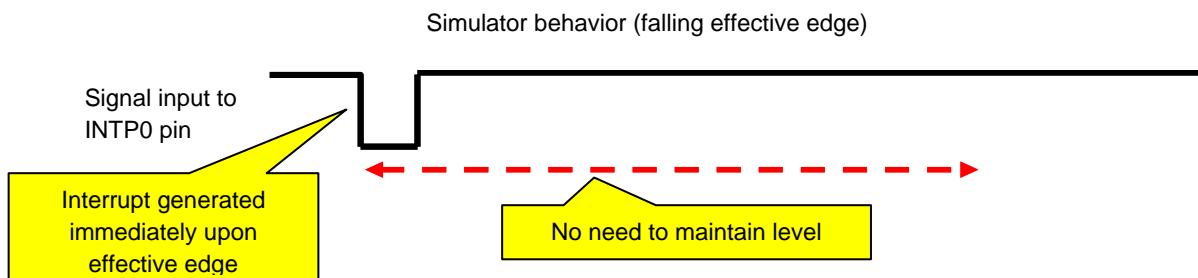
The simulator does not simulate the noise reduction circuit. For example, if you input the active level to an external-interrupt pin with a noise reduction circuit, the interrupt will be received even if the active-level amplitude is too low.

The example below considers the case when there is input to the INTP0 pin.

There is a noise reduction circuit on the INTP0 pin of the target device. For this reason, in order to generate an interrupt, it is necessary to input an effective edge to the target device, and subsequently maintain the signal level. (See the user's manual of the target device for the length of time it must be maintained.)



In the case of the simulator, however, this noise reduction circuit is not simulated. For this reason, an interrupt will be generated any time a valid edge is generated. (No need to maintain signal level).



### 5.1.7 DMA controller

The transfer speeds of the target device and simulator differ as follows when simulating the DMA controller.

[Target device]

- \* The time required for a DMA transfer is: DMA response time + memory access time of transfer source + 1 clock cycle + memory access time of transfer destination.
- \* If there is a contention of DMA transfer timing between CPU bus access and DMA bus access by another channel, then the bus access with the lower priority waits until the bus access with the higher priority completes.

[Simulator]

- \* It takes zero clock cycles to complete one DMA transfer.
- \* If there is a contention of DMA transfer timing between CPU bus access and DMA bus access by another channel, then the bus accesses are performed simultaneously.

### 5.1.8 External bus interface functions

Some of the external bus interface functions can be simulated, and some cannot.

[Functions that can be simulated]

- \* ROM and RAM connection
- \* Access to connected ROM/RAM

[Functions that cannot be simulated]

- \* External bus-related SFR simulation (External bus access is possible even without configuring SFR.)
- \* Check signal input to external bus pins in the Timing Chart window  
(It will appear as high impedance.)
- \* Input to WAIT or HLDRQ pin (It will be ignored.)
- \* Access Speed (always 0 clock)

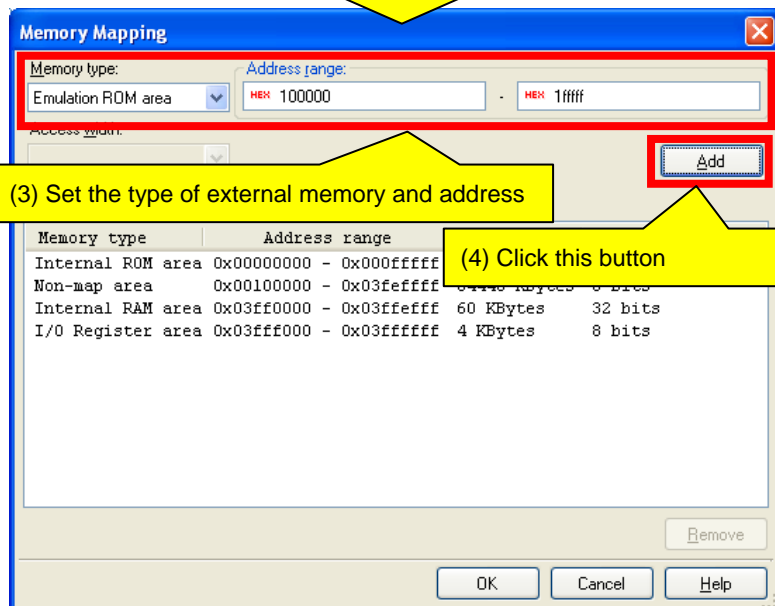
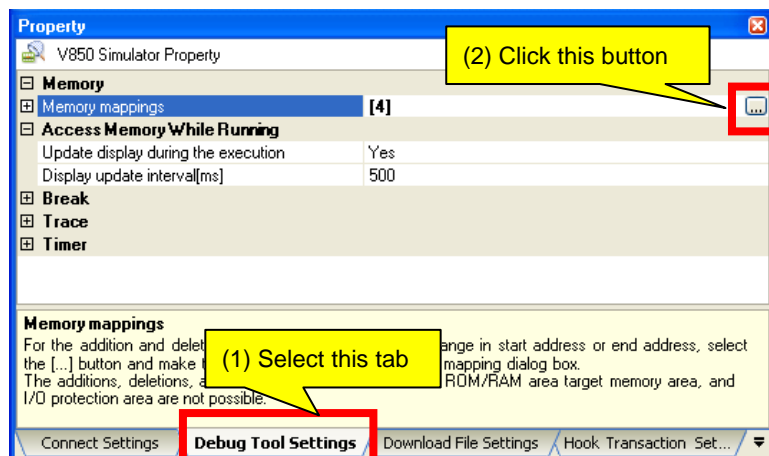
When connecting ROM or RAM to the external bus, perform configuration in the Property panel, from the Debugging Tool Setting tab.

Connect by entering:

- \* Type of memory to connect to (emulation ROM area or emulation RAM area)
- \* Memory address to connect to

This setting enables both:

- \* Writing to external bus
- \* Reading from external bus



### 5.1.9 Noise filter on asynchronous serial interface A (UARTA)

Although the target device's asynchronous serial interface A (UARTA) has a noise filter to reduce noise on the input pin, the simulator does not simulate this. Since there is no noise in the simulator's signal, it would be meaningless to simulate this function.

### 5.1.10 Baud rate of asynchronous serial interface (UARTA, UARTB<sup>Note</sup>)

If the baud rate of the asynchronous serial interface A (UARTA) or B (UARTB) is set to 233 bps or lower, operation will be abnormal (it will operate at a higher baud rate than the one set). Do not specify a baud rate that is 233 bps or lower.

Note: SJ3-H, SK3-H only

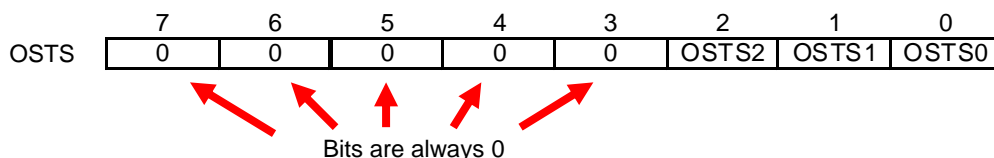
### 5.1.11 Baud rate clock input of asynchronous serial interface A (UARTA)

Although the target device's asynchronous serial interface A (UARTA) has an ASCKA0 pin as a baud rate clock input pin, the simulator does not simulate this. Inputs of baud rate clocks to this pin are ignored.

### 5.1.12 Constant 0/1 bits of I/O registers

The I/O register has bits that are always 0 or 1.

For example, bits 3 to 7 are always 0 for the oscillation stabilization time selection register (OSTS).



Although the values of these bits cannot be changed from the target device, the values can be changed from the simulator. Note that changing these values has no effect on behavior.

### 5.1.13 Stabilization time of A/D converter

The simulator does not simulate the stabilization time of the A/D converter. This causes the following differences in behavior.

[Time from start to end of A/D conversion on target device]

- \* Normal conversion mode: stabilization time + conversion time + wait time
- \* High-speed conversion mode: stabilization time + conversion time
- \* Continuous conversion mode: stabilization time + conversion time (first conversion), conversion time (second and subsequent conversions)

[Time from start to end of A/D conversion on simulator]

- \* Normal conversion mode: conversion time + wait time
- \* High-speed conversion mode: conversion time
- \* Continuous conversion mode: conversion time

#### 5.1.14 Default voltage of AV<sub>REF0</sub> pin and AV<sub>REF1</sub> pin

Default voltage of AV<sub>REF0</sub> pin is 3.3V. And default voltage of AV<sub>REF1</sub> pin is 3.6V.

Note : The meaning of "Default voltage " is the voltage when the pin have no connection.

#### 5.1.15 Capture trigger of 16-bit timer/event counter Q (TMQ)

Because the simulator does not support the CAN controller, do not set the following as the capture trigger for 16-bit timer/event counter Q (TMQ). If one of these settings is made, the capture trigger will not be activated.

- \* Selection of CAN0's TSOUT signal as TIQ02 pin input signal  
(Set ISEL0 bit of selector operation control register 0 (SELCNT0) to 1)
- \* Selection of CAN1's TSOUT signal as TIQ03 pin input signal  
(Set ISEL1 bit of selector operation control register 0 (SELCNT0) to 1)

#### 5.1.16 Interrupt response time

The interrupt response times of the target device and simulator differ.

[Target device]

It takes at least 4 clock cycles after an interrupt is generated until execution branches to the handler address.

[Simulator]

Execution branches to the handler address immediately upon the interrupt.

#### 5.1.17 Low-voltage detector

The simulator does not simulate the internal RAM data status register (RAMS). Although the initial value will be the same as the target device (0x01), the behavior differs on the following three points.

- \* Writing is possible without a specific sequence.
- \* The RAMF bit will not be set to 1 if a voltage below the RAM hold voltage is detected.
- \* Setting the EVARAMIN bit of peripheral emulation register 1 (PEMU1) to 1 will not cause the RAMF bit to be set to 1.

#### 5.1.18 Chip select control function (SJ3-H, SK3-H only)

The simulator does not simulate the chip select control function by the chip area select control registers 0, 1 (CSC0 and CSC1).

#### 5.1.19 Frequency modulation of clock generation (SJ3-H, SK3-H only)

The simulator does not simulate the frequency modulation, the frequency modulation ratio, and the frequency cycle in SSCG mode.

### 5.1.20 FIFO mode of asynchronous serial interface B (SJ3-H, SK3-H only)

The simulator does not simulate the pending mode of the transmission enable interrupt request signal (INTUBnTIT) and the reception completion interrupt request signal (INTUBnTIR) in FIFO mode. The simulator operates same as in pointer mode.

## 5.2 Notes for using simulator GUI

### 5.2.1 Cautions for controlling each windows


The following keyboard operations are not available in the simulator windows (signal-data editor window, I/O panel window, and serial window).


- \* Navigation via tab or arrow keys (←, ↑, →, ↓)
- \* Deletion via the Del or Backspace keys
- \* Copy & paste and other operations via the Ctrl + C, V, X, A, or Z keys.

Perform the above operations as follows.

- \* Navigation:           Navigate using the mouse.
- \* Deletion:            Right click and perform the action via the context menu.
- \* Copy & paste, etc.: Right click and perform the action via the context menu.

### 5.2.2 Cautions for closing simulator GUI window

The simulator GUI window can only be closed by disconnecting from the debugging tool, or by closing CubeSuite+ proper. (The  button cannot be clicked.)

Additionally, although it appears that the  button can be pressed if Aero is enabled in Windows Vista, pressing this button will not close the GUI window.

### 5.2.3 Cautions for showing help for the simulator GUI window

Pressing the F1 key in the simulator GUI window will not display the help if none of the internal windows are visible (e.g. the I/O panel window).

To display the help for the simulator GUI window, from the GUI window's menu, select [Help] > [Main Window].

## 5.2.4 Cautions for disconnecting the debug tool

CubeSuite+ may exit if the debugging tool is disconnected while any of the following dialog boxes is open from the simulator GUI window. Make sure that the following dialog boxes are closed before disconnecting the debugging tool.

- Save As
- Open
- New
- Color
- Font
- Customize
- Loop
- Select Pin
- Search Data
- Format (UART)
- Format (CSI)
- Message (e.g. Error)
- Parts Button Properties
- Analog Button Properties
- Parts Key Properties
- Parts Level Gauge Properties
- Parts Led Properties
- Parts Segment LED Properties
- Parts Matrix Led Properties
- Parts Buzzer Properties
- Pull up / Pull down
- Entry Bitmap
- Object Properties

## 5.2.5 Cautions for setting the Host Machine's language and region

If a Japanese OS is installed on your Host Machine, then if the language or region is set to other than Japanese/Japan, the menus and dialog-box names of the simulator GUI window will be shown in English. Similarly, if a non-Japanese OS is installed on your Host Machine, then if the language or region is set to Japanese/Japan, the menus and dialog-box names of the simulator GUI window will be shown in Japanese.

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