User's Manual

E1/E20 Emulator

Additional Document for User's Manual (Notes on Connection)

Supported Devices:
V850E2M, V850E2S

Renesas Electronics
www.renesas.com

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Contents

1. Outline

1.1 Features

E1/E20 Emulator is an on-chip debug emulator with flash programming function, which is used for debugging and programming a program to be embedded in on-chip flash memory microcontrollers. This product can debug with the target microcontroller connected to the target system, and can write programs to the on-chip flash memory of microcontrollers.

1.2 Cautions on Using E20

The functions used for debugging of the V850E2M, V850E2S device by using the E20 are the same as in the E1. Large trace function, characteristic functions of the E20, cannot be used. The power supply function from the E20 is not supported.

1.3 Configuration of Manuals

Documentation for the E1/E20 emulator manual is in two parts: the E1/E20 Emulator User's Manual and the E1/E20 Emulator Supplementary Document for the User's Manual (this manual). Different versions of the latter correspond to different sets of MCUs. Be sure to read both of the manuals before using the E1/E20 emulator (hereinafter referred to as "the emulator").

(1) The E1/E20 emulator user's manual has the following contents:

- Components of the emulators
- Emulator hardware specification
- Connection to the emulator and the host computer and user system

(2) The E1/E20 Emulator Supplementary Document for the User's Manual has the following contents:

- For use in hardware design, an example of connection and the interface circuit required to connect the emulator.
- Notes on using the emulator

2. Designing the User System

To connect the E1/E20 emulator (hereinafter referred to as the emulator), a connector for the user system interface cable must be mounted on the user system. When designing the user system, read this section of this manual and the hardware manual for the MCUs.

2.1 Connecting the Emulator with the User System

Table 2-1 shows the type numbers of the E1/E20 emulators

Table 2-1 Type Numbers

	Type Number	Manufacturer	仕様
14-pin Connector	7614-6002	Sumitomo 3M Limited	14-pin straight type (Japan)
	2514-6002	3M Limited	14-pin straight type (other countries)

Figures 2.1 show examples of the connection between a user system interface cable of the 14-pin type. Do not mount other components with a height exceeding 10 mm within 5 mm of the connector on the user system. 38-pin of the E20 is not supported. To use the E20, use the 38-pin/14-pin conversion adapter [R0E000200CKA00] that comes with the E20 for connection.

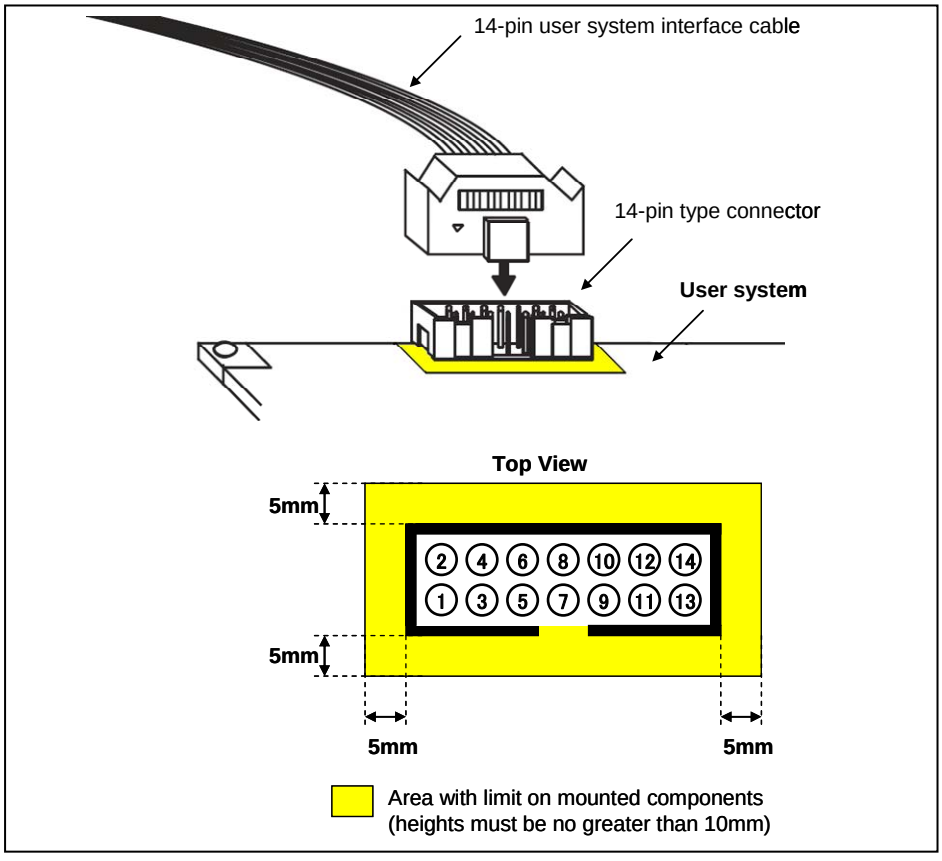


Figure 2-1 Connecting the User System Interface Cable to the 14-pin Connector of the E1/E20 Emulator

2.2 Pin Assignments of the Connector on the User System

Table 2-2 shows the pin assignments of the 14-pin connectors.

Table 2-2 Pin assignments of the connector (14-pin)

Pin No	Signal (# : Low Active)			Input/ Output [Note3]
	JTAG	UART (Programming & Srial OCD)	CIS (Programming)	
1	TCK	-	FPCK	Input
2 [Note1]	GND	GND	GND	-
3	TRST#	-	-	Input
4	-	FLMD0	FLMD0	Input
5	TDO	-	FPDT	Output
6	-	RESET_IN#	-	Output
7	TDI	FPDR	FPDR	Input/Output
8	VDD	VDD	VDD	-
9	TMS	-	-	Input
10	-	RESET_OUT# [Note2]	RESET_OUT# [Note2]	Input
11	RDY#	-	-	Output
12 [Note1]	GND	GND	GND	-
13	RESET_OUT#	RESET_OUT# [Note2]	RESET_OUT# [Note2]	Input
14	GND	GND	GND	-

Notes 1. Securely connect pins 2, 12, and 14 of the connector to GND of the user system. These pins are used for electrical grounding as well as for monitoring of connection with the user system by the E1/E20.

2. Securely connect both pin 10 and pin 13. These pins are also used to monitor the user system.

3. Input to or output from the user system

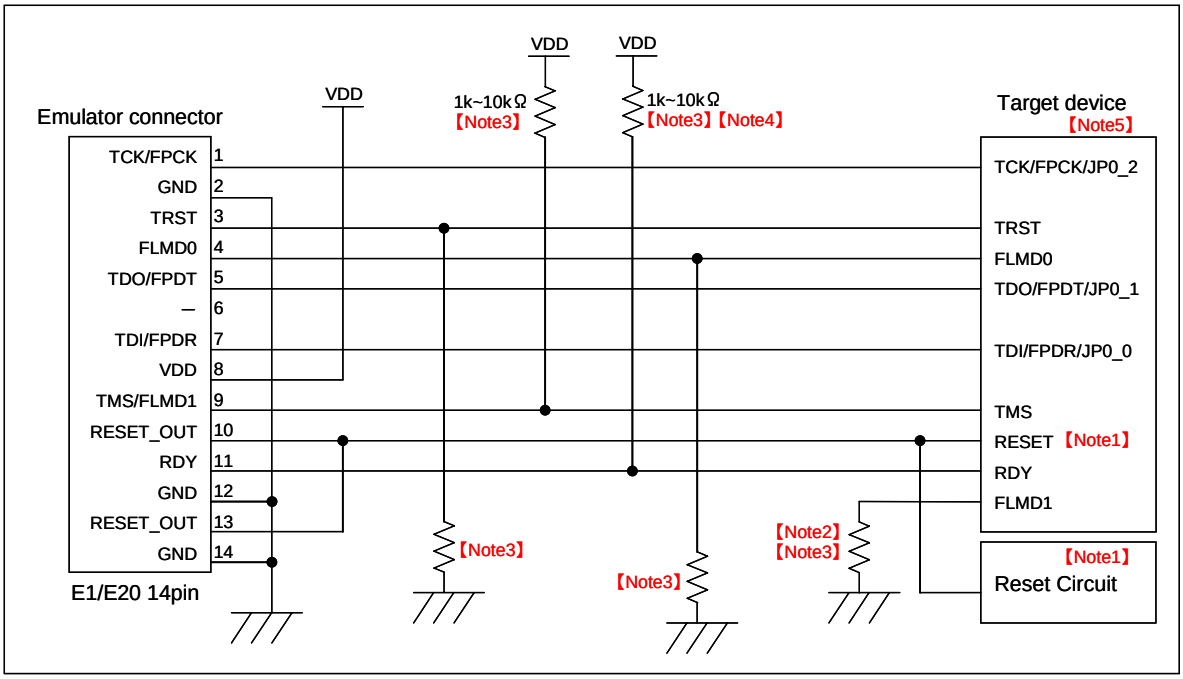
2.3 Recommended Circuit between the Connector and the MCU

This section describes recommended circuits for connection between the 14-pin connector and the MCU.

2.3.1 Recommended Circuit

There are 5 types of recommended circuit for each purpose. Select the relevant circuit for the purpose. Be sure to take into consideration the specifications of the target device as well as measures to prevent noise when designing your circuit.

Purpose	Figure
Debugging(JTAG) and programming(CSI)	Figure 2-2
Only debugging(JTAG)	Figure 2-3
Only programming(CSI)	Figure 2-4
Debugging(UART) and programming(UART)	Figure 2-5
Only programming(UART)	Figure 2-6

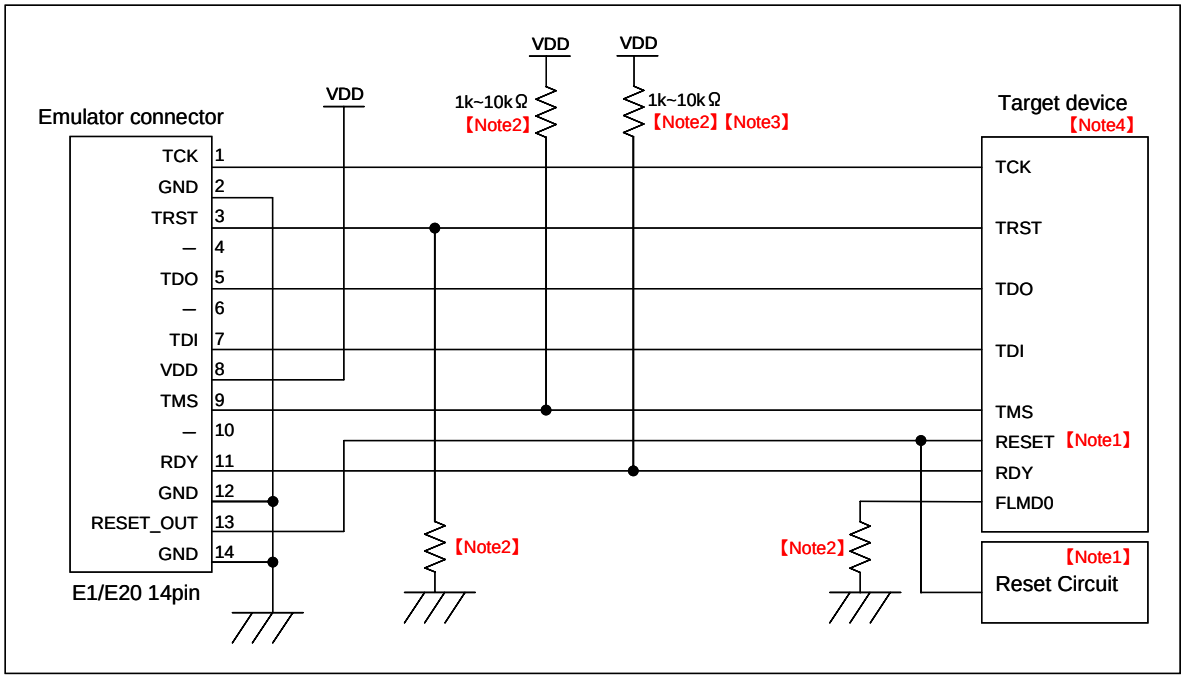


【Caution】Wiring patterns between the connector and the MCU must be as short as possible

Figure 2-2 Recommended Circuit (debugging(JTAG) and programming(CSI))

【Note】1. This circuit is designed assuming that RESET signal is output from the N-ch open-drain buffer. For details, refer to 2.3.2.

2. This signal must be set at low level when resetting.
   In case of using alternate functions, make sure not to be high level when reset.
3. Refer to the data sheet of MCU regarding register.
4. Emulator must be designed to be isolated when it is not in use by switch, etc.
5. Pin name differs according to the data sheet of MCU.
   Refer to those the data sheet of MCU to find an actual pin name.



【Caution】Wiring patterns between the connector and the MCU must be as short as possible

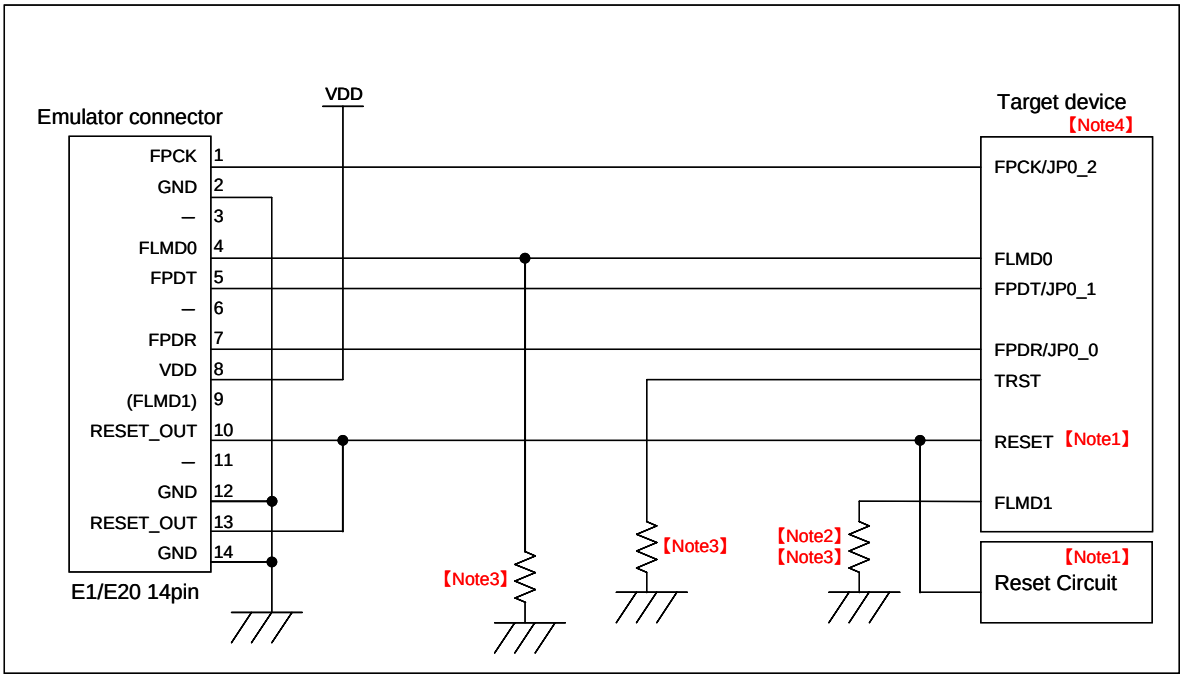
Figure 2-3 Recommended Circuit (only debugging(JTAG))

【Note】1. This circuit is designed assuming that RESET signal is output from the N-ch open-drain buffer. For details, refer to 2.3.2.

2. Refer to the data sheet of MCU regarding register.

3. Emulator must be designed to be isolated when it is not in use by switch, etc.

4. Pin name differs according to the data sheet of MCU.
Refer to those the data sheet of MCU to find an actual pin name.

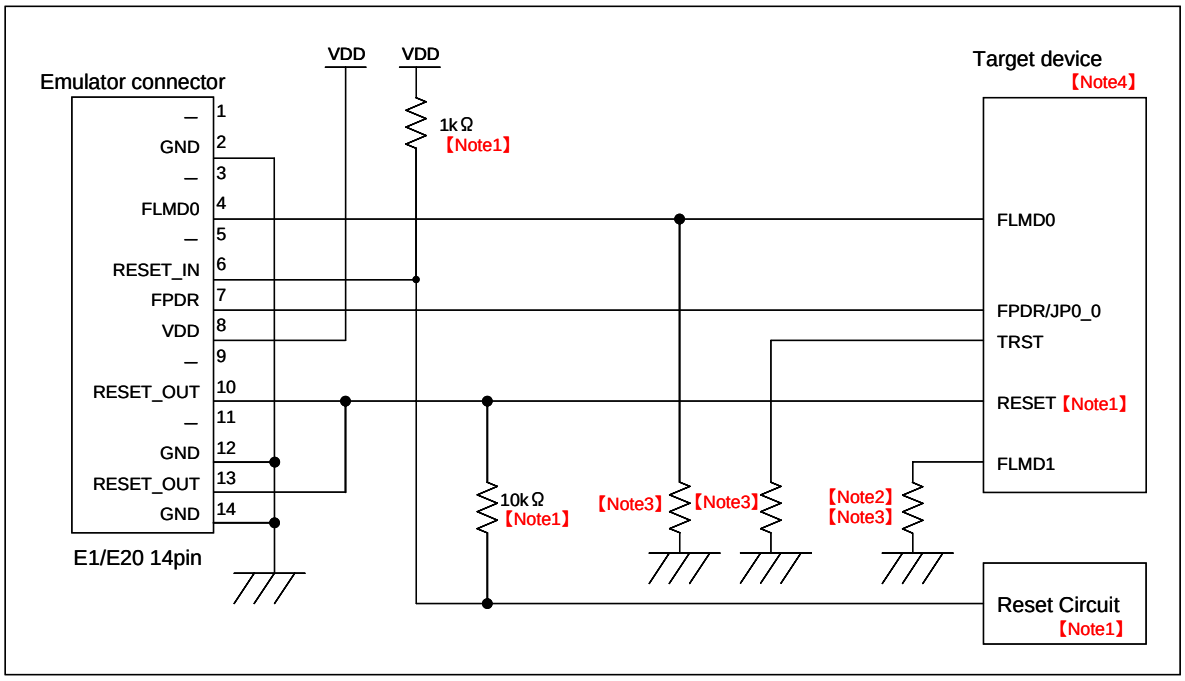


【Caution】Wiring patterns between the connector and the MCU must be as short as possible

Figure 2-4 Recommended Circuit (only programming(CSI))

【Note】1. This circuit is designed assuming that RESET signal is output from the N-ch open-drain buffer. For details, refer to 2.3.2.

2. This signal must be set at low level when resetting.
   In case of using alternate functions, make sure not to be high level when reset.
   In case of using alternate function pin with pull-up resister, connect to FLMD1 of emulator. High level is output from the emulator when flash programming.
3. Refer to the data sheet of MCU regarding register.
4. Pin name differs according to the data sheet of MCU.
   Refer to those the data sheet of MCU to find an actual pin name.

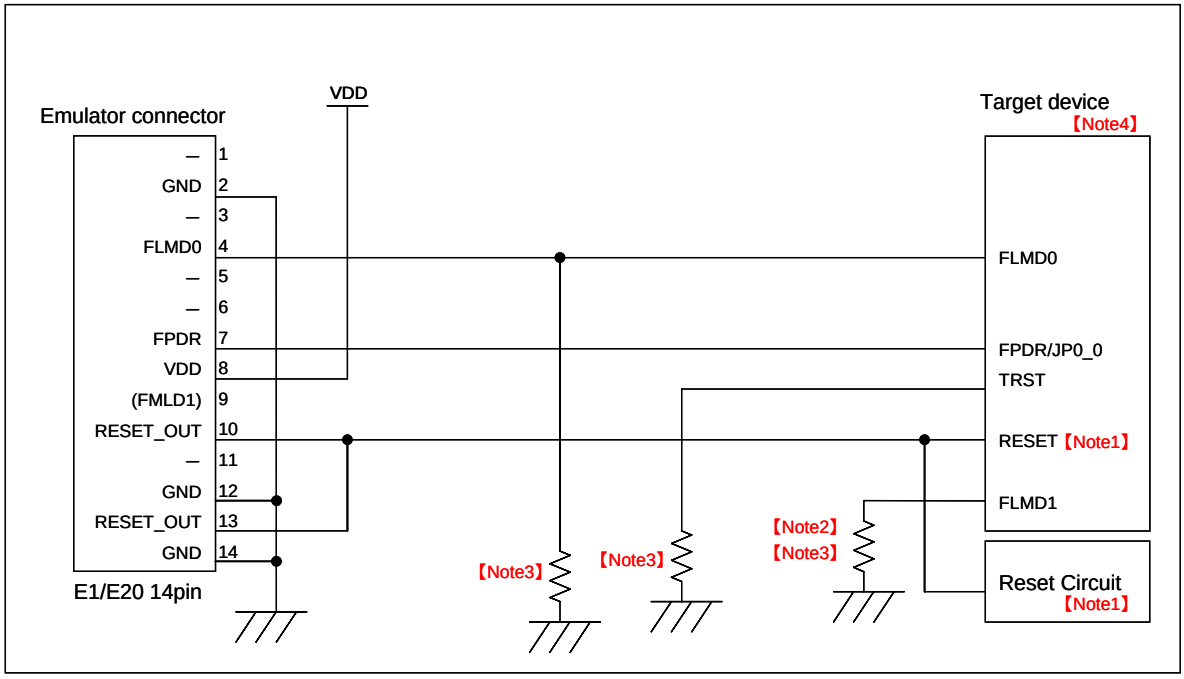


【Caution】Wiring patterns between the connector and the MCU must be as short as possible

Figure 2-5 Recommended Circuit (debugging(UART) and programming(UART))

【Note】1. This circuit is designed assuming that RESET signal is output from the N-ch open-drain buffer. For details, refer to 2.3.2.

2. This signal must be set at low level when resetting.
   In case of using alternate functions, make sure not to be high level when reset.
3. Refer to the data sheet of MCU regarding register.
4. Pin name differs according to the data sheet of MCU.
   Refer to those the data sheet of MCU to find an actual pin name.



【Caution】Wiring patterns between the connector and the MCU must be as short as possible

Figure 2-6 Recommended Circuit (only programming(UART))

【Note】1. This circuit is designed assuming that RESET signal is output from the N-ch open-drain buffer. For details, refer to 2.3.2.

2. This signal must be set at low level when resetting.
   In case of using alternate functions, make sure not to be high level when reset.
   In case of using alternate function pin with pull-up resister, connect to FLMD1 of emulator. High level is output from the emulator when flash programming.

3. Refer to the data sheet of MCU regarding register.

4. Pin name differs according to the data sheet of MCU.
   Refer to those the data sheet of MCU to find an actual pin name.

2. 3. 2 Regarding Connection of RESET

Connect the RESET signal as shown in Figure 2-7 if any of the conditions listed below is satisfied. The connection of reset is necessary to rewrite the flash memory. When one of the following conditions is satisfied, leave open the pin for the RESET signal that is output from the E1/E20 emulator.

- The target device should be kept in the reset state before debugger startup or after debugger termination.
- E1/E20 emulator is used for flash programming.
- Serial OCD is used.

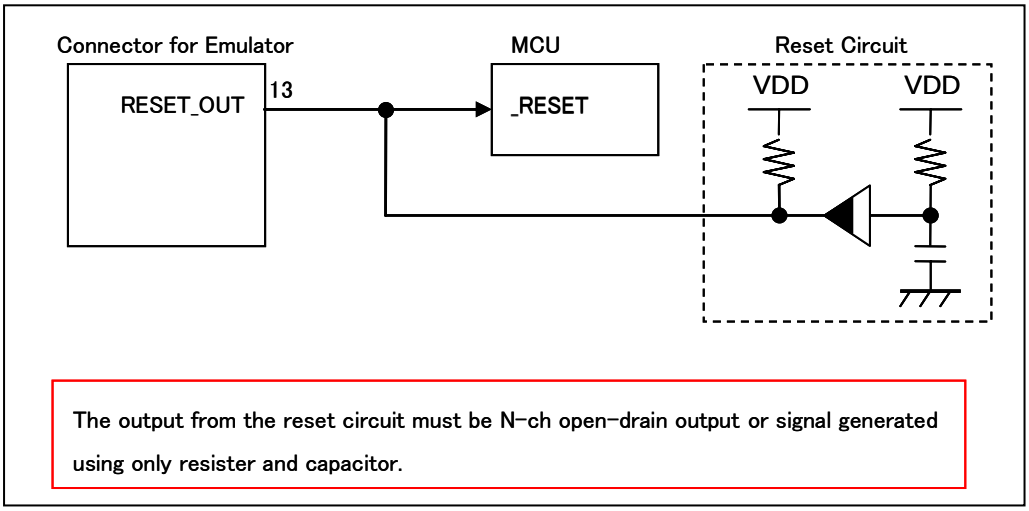


Figure 2-7 Reset circuit in case of JTAG connection

2. 3. 3 Caution of hot plug-in function

As shown at Figure 2-8, because 4.7uF capacitor is fixed with 8th pin of E1/E20 emulator inside, power supply voltage in user system may decrease for an instant when it is in hot-plug connecting. This decrease in voltage might lead MCU to be reset.

By fixing Ferrite Beads (or inductor) and large-sized low ESR capacitor with an area close to VDD line of debug connector ,as shown at Figure 2-9, it is able to reduce the value of the voltage to the minimum. However, it is not the solution that completely prevent it.

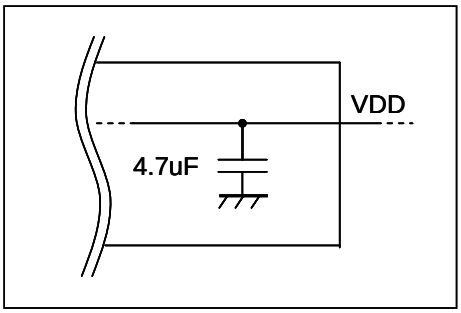


Figure 2-8 E1/E20 Emulator Internal circuit

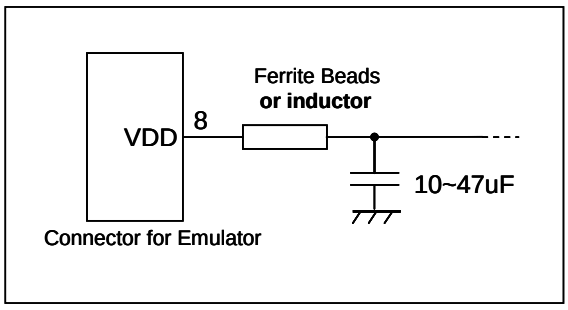


Figure 2-9 The measure method of E1 Emulator

3. Securing of debug resources for Serial OCD I/F

When Serial OCD I/F use, the user must prepare the following to perform communication between E1/E20 Emulator and the target device. Refer to the descriptions on the following pages and set these items in the user program or using the compiler options. When using JTAG interface, the setting of this section is needless.

- Modification of reset vector
- Securing of memory area
- Securing of serial interface for communication

3.1 Reset handler

A reset handler includes the jump instruction for the debug monitor program.

[How to secure areas]

It is not necessary to secure this area intentionally. When downloading a program, however, the debugger rewrites the reset vector in accordance with the following cases. If the rewritten pattern does not match the following cases, the debugger generates an error.

• When three nop instructions are placed in succession from address 0

Before writing		After writing
0x0 nop	→	Jumps to debug monitor program at 0x0
0x2 nop		
0x4 nop		
0x6 xxxx		0x6 xxxx

• When three 0xFFFF are successively placed from address 0 (already erased device)

Before writing		After writing
0x0 0xFFFF	→	Jumps to debug monitor program at 0x0
0x2 0xFFFF		
0x4 0xFFFF		
0x6 xxxx		0x6 xxxx

• The jr instruction is placed at address 0 (when using Renesas Electronics compiler CX)

Before writing		After writing
0x0 jr disp22	→	Jumps to debug monitor program at 0x0
0x4 xxx		
0x6 xxx		0x6 jr disp22 – 6

• mov32 and jmp are placed in succession from address 0 (when using IAR compiler ICCV850)

Before writing		After writing
0x0 mov imm32,reg1	→	Jumps to debug monitor program at 0x0
0x6 jmp [reg1]		0x6 mov imm32,reg1
		0xc jmp [reg1]

• The jump instruction for the debug monitor program is placed at address 0

Before writing		After writing
Jumps to debug monitor program at 0x0	→	No change

3.2 Securing of memory area

The shaded portions in Figure 3-1 are the areas reserved for placing the debug monitor program, so user programs and data cannot be allocated in these spaces. These spaces must be secured so as not to be used by the user program.

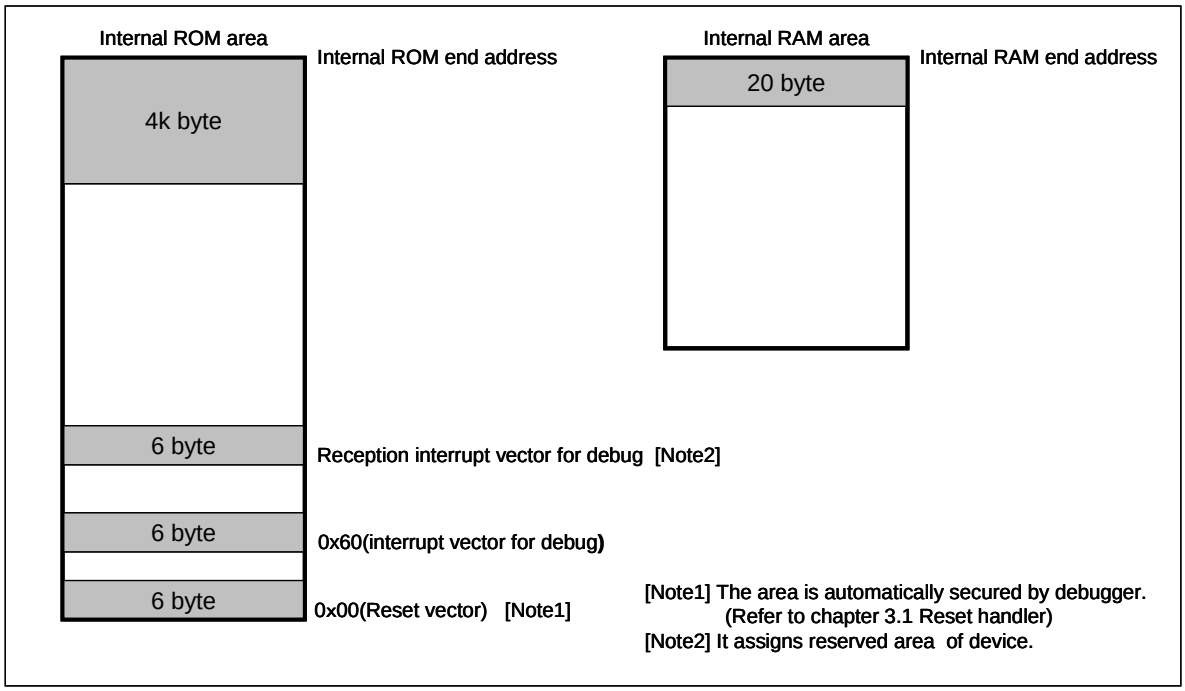


Figure 3-1 Memory Spaces Where Debug Monitor Programs Are Allocated

3.3 Securing of serial interface for communication

Securing of serial interface for communication settings related to the serial interface modes are performed by the debug monitor program, but if the setting is changed by the user program, a communication error may occur.
To prevent such a problem from occurring, communication serial interface must be secured in the user program.
Settings other than below are prohibited.
Do not change bit 0, an initial value, of each register in port group JP0 which is not described in below.

[Port Group JP0]

1. Port IP control register [JPIPC0] x:Any

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0

2. Port bi-direction control register [JPBDC0]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1

3. Port open drain control register [JPODC0]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1

4. Port function control expansion register [JPFCE0]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1

5. Port function control register [JPFC0]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1

6. Port mode control register [JPMC0]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1

7. Port mode register [JPM0]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0

8. Pull-up option register [JPU0]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1

4. Specifications

Specifications are below table.

Large Item	Middle Item	Small Item	Specification
Hardware Common	Target host machine		Computer equipped with a USB port OS is due to the software tool.
	User system interface		14-pin connector
	Host machine interface		USB2.0 (Full speed/ High speed)
	Connection to the user system		Connection by the provided user-system interface cable
	Power supply function (E1 Emulator used)		3.3V or 5.0V, set in software tool, can be supplied to the user system (with current up to 200 mA)
	Power supply for the emulator		No need (the host computer supplies power through the USB)
Related debugging	Break	Software break	ROM area :8 points RAM area :2000 points
		Hardware break	4 points (commonly used by execution and access)
		Forced break	Available
	Event	Number of events	4 points (commonly used by execution and access)
		Available function	Only hardware break
		Combination of events	OR, sequential
	Trace		Unavailable
	Performance measurement	Measurement item	From run to break
		Performance	JTAG: Resolution 100ns, Max. measurement time 7 minutes (During TCK is 10MHz) Serial OCD: Resolution 100us, Max. measurement time 100 hours
	Real-time RAM monitor		Available (the bus is used when monitoring)
	Direct memory modification		Available (the bus is used when monitoring)
	Debugging console		Unavailable
	Downloading to external flash memory		Available (Depends on Software)
	Hot plug-in		Available Note
	Security		12-byte ID code authentication
Related programming	Clock supply		16, 8, or 4 MHz clock can be supplied Clock mounted on the target system can be used
	Security flag setting		Available
	Standalone operation		Unavailable (must be connected to host machine)

Note: To use the hot plug-in function with the E1 emulator, please purchase the separately available hot-plug adapter(R0E000010ACB00).

5. Notes on Usage

Make sure to notes on usage in this section.

5.1 Lists

Table 5-1 Lists of notes on usage

No	Item
1	Handling of device that was used for debugging
2	When breaks cannot be executed [Serial OCD used]
3	When pseudo real-time RAM monitor (RRM) function and DMM function do not operate [Serial OCD used]
4	Standby (HALT mode, STOP mode, DEEPSTOP mode) release [Serial OCD used]
5	Writing to peripheral I/O registers that requires a specific sequence, using DMM function
6	Flash self programming
7	Operation after reset [Serial OCD used]
8	Debugging with real machine running without using E1/E20 Emulator [Serial OCD used]
9	Alternate functions
10	Regarding current consumption
11	Regarding setting of power-save mode
12	Regarding WAKE pin
13	Regarding PWGD pin
14	Regarding POC function and emulation of turning OFF
15	Regarding ECC errors
16	When high-speed internal oscillator (High-speed IntOsc) is stopped
17	Regarding Iso0, Iso1 area
18	During break
19	Regarding hardware breaks in embedded RAM area
20	Writing quality of flash programming

5.2 Details

No.1 Handling of device that was used for debugging

Description: Do not mount a device that was used for debugging on a mass-produced product, because the flash memory was rewritten during debugging and the number of rewrites of the flash memory cannot be guaranteed. When the flash memory can not be rewritten, the software tool generates the error. In case of that, change the mounted device.

No.2 When breaks cannot be executed [Serial OCD used]

Description: Forced breaks cannot be executed if the following condition is satisfied.

- Interrupts are disabled (DI)

No.3 When pseudo real-time RAM monitor (RRM) function and DMM function do not operate [Serial OCD used]

Description: The pseudo RRM function and DMM function do not operate if one of the following conditions is satisfied.

- Interrupts are disabled (DI)
- Clock different from the one specified in the debugger is used for communication

No.4 Standby (HALT mode, STOP mode, DEEPSTOP mode) release [Serial OCD used]

Description: The standby mode is released if one of the following conditions is satisfied.

- With pseudo RRM and DMM functions enabled [Serial OCD used]
- On generation of a break

No.5 Writing to peripheral I/O registers that requires a specific sequence, using DMM function

Description: Peripheral I/O registers that requires a specific sequence cannot be written with the DMM function.

No.6 Flash self programming

Description: If a space where the debug monitor program is allocated is rewritten by flash self programming, the debugger can no longer operate normally.
Do not break in ROM area during flash environment.

No.7 Operation after reset [Serial OCD used]

Description: After an external pin reset or internal reset, the monitor program performs debug initialization processing.
Consequently, the time from reset occurrence until user program execution differs from that in the actual device operation.

No.8 Debugging with real machine running without using E1/E20 Emulator [Serial OCD used]

Description: If debugging is performed with a real machine running, without using E1/E20 emulator, write the user program using RFP(Renesas Flash Programmer). Programs downloaded by the debugger include the monitor program, and such a program malfunctions if it is not controlled via E1/E20 Emulator.

No.9 Alternate functions

Description: The alternate functions of these pins cannot be used during on-chip debugging. And be careful not to conflict the signals from emulator while the flash programming is operating.

No.10 Regarding current consumption

Description: The current consumption in the target device increases during debugging compared with that in normal operation mode, because the OCD unit of the target device operates during debugging.

No.11 Regarding setting of power-save mode

Description: When setting isolated area 0 (Iso0) and isolated area 1 (Iso1) to power-save mode, clear the wake-up factor mask of Iso0 (WUPMSKH0-WUPMSKH015) and Iso1 (WUPMSKH1-WUPMSKH115) before setting power-save mode.
When setting only Iso1 to power-save mode, clear the wake-up factor mask (WUPMSKH1-WUPMSKH115) before setting power-save mode.

No.12 Regarding WAKE pin

Description: WAKE pin becomes high level during external reset and DEEPSTOP due to the device.

No.13 Regarding PWGD pin

Description: When the PWGD pin is not used, lock it to H.
Even if option byte PWGDEN is 0, the PWGD pin is treated as H at all times when not in use.

No.14 Regarding POC function and emulation of turning OFF

Description: Make sure that the power to the target system is not shut down during debugging. Regarding to check the operation of POC function and tuning OFF, perform without the emulator. In case the user system is turning OFF instantaneously, the debugger may hang up.

No.15 Regarding ECC errors

Description: When a program is downloaded and executed, E1/E20 emulator uses flash self programming, and it initializes the onboard RAM area to that an ECC error does not occur. For this reason, ECC errors cannot be emulated after downloading a program.

No.16 When high-speed internal oscillator (High-speed IntOsc) is stopped

Description: If a break occurs while the high-speed IntOsc is stopped, the debugger may hang. A reset must be performed in order to recover.

No.17 Regarding Iso0, Iso1 area

Description: The power of Iso0, Iso1 is not dropped by internal reset, external reset and DEEPSTOP when debugging (the value of RAM is held).

No.18 During break

Description: Do not generate a reset via a pin reset while the program is stopped (during a break). Doing so may cause the debugger to hang.

No.19 Regarding hardware breaks in embedded RAM area

Description: If a hardware break is set in the embedded RAM area, the break occurs on a match with the low-order address. As shown in the example below, the break may occur at an unintended location.
Example: When a break is set at 0x0FED_C000H, breaks will occur at the following addresses.
0x01ED_C000H, 0x03ED_C000H, 0x05ED_C000H, 0x07ED_C000H, 0x09ED_C000H, 0x0BED_C000H, 0x0DED_C000H

No.20 Writing quality of flash programming

Description: To improve the writing quality, fully understand, verify, and evaluate the following items before using E1 emulator.

- Circuits are designed as described in the user's manuals for the device and E1/E20 emulator.
- The device, E1/E20 emulator and the software are used as described in each user's manual.
- The power supplied to the target system is stable.

E1/E20 Emulator
Additional Document for User's Manual (Notes on Connection)

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Colophon 1.1

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