

5.3.3 Bit Synchronous Mode

Error Checking

- Underrun error ... page 303

(Current)

Usage Note:

Data (1 to 4 bytes) written into the transmit buffer by the MPU or DMAC at the same time as underrun occurs may be left in the transmit buffer, and not transmitted, depending on the write timing. When data is next written to the transmit buffer by the MPU after clearing the UDRN bit, or data is transferred by the DMAC, the remaining data will be added at the head of the next frame, and transmitted.

To prevent this, use TBN to check the number of data bytes in the transmit buffer after underrun occurs. If there is data left in the transmit buffer, issue a transmit buffer clear command.

(Corrected)

Usage Note:

Data (1 to 4 bytes) written into the transmit buffer by the MPU or DMAC at the same time as underrun occurs may be left in the transmit buffer, and not transmitted, depending on the write timing. When data is next written to the transmit buffer by the MPU after clearing the UDRN bit, or data is transferred by the DMAC, the remaining data will be added at the head of the next frame or the remaining data and next frame combine into one frame, and transmitted.

To prevent this, TXINTE bit of Interrupt Enable Register 0 (IE0) and UDRNE bit of Interrupt Enable Register 1 (IE1) set to 1. If an interrupt request is generated by the underrun occurs, please issue the command as following.

- (1) TX disable B command.
- (2) Transmit Buffer Data Number Register (TBN) to check the number of data bytes in the transmit buffer.
- (3) TX buffer clear command.
- (4) TX enable command.

5.3.4 Transparent Mode

Error Checking

- Underrun error ... page 309

(Current)

An underrun error occurs if the $\overline{\text{SYNCO}}$ pin is low and the transmit buffer is empty.

When underrun is detected, the UDRN bit is set to 1 in status register 1 (ST1), and the TXRDY bit is cleared to 0 in status register 0 (ST0). When the UDRN bit is set to 1, an interrupt request is generated, if enabled. The UDRN bit is cleared to 0 only when a 1 is written to the bit position or ST1 is reset.

(Corrected)

An underrun error occurs if the $\overline{\text{SYNCO}}$ pin is low and the transmit buffer is empty.

When underrun is detected, the UDRN bit is set to 1 in status register 1 (ST1), and the TXRDY bit is cleared to 0 in status register 0 (ST0). When the UDRN bit is set to 1, an interrupt request is generated, if enabled. The UDRN bit is cleared to 0 only when a 1 is written to the bit position or ST1 is reset.

Usage Note:

Data (1 to 4 bytes) written into the transmit buffer by the MPU or DMAC at the same time as underrun occurs may be left in the transmit buffer, and not transmitted, depending on the write timing. When data is next written to the transmit buffer by the MPU after clearing the UDRN bit of Status Register 1 (ST1), or data is transferred by the DMAC, the remaining data will be added at the head of the next frame or the remaining data and next frame combine into one frame, and transmitted.

To prevent this, TXINTE bit of Interrupt Enable Register 0 (IE0) and UDRNE bit of Interrupt Enable Register 1 (IE1) set to 1. If an interrupt request is generated by the underrun occurs, please issue the command as following.

- (1) TX disable B command.
- (2) Transmit Buffer Data Number Register (TBN) to check the number of data bytes in the transmit buffer.
- (3) TX buffer clear command.
- (4) TX enable command.