

Standard Linear IC

Reliability

The importance of semiconductor devices continues to increase due to the increasing performance and scale of electronic systems. We at Renesas Technology Corp., are continually striving to maintain and improve the reliability of our semiconductor devices through the accumulation of unflagging efforts. We have been providing high-quality semiconductor devices to a wide range of electronics fields under a harmonious quality assurance system that includes not only process technologies and individual designs to respond to our users requests, but also the whole process from planning and development to after-service.

This section presents reliability data, notes on device handling, and other points so that Renesas semiconductor devices can be used with high reliability. For more details, see the "Renesas Semiconductor Device Reliability Handbook."

1. Reliability Data

This section presents failure criterion and the latest reliability test results.

1.1 Failure Criterion

Table 1 lists the failure criterion for linear IC reliability testing. While the test items and test conditions differ with the product type, the criterion are based on this table.

Table 1 Linear IC Failure Criterion

	Item	Failure Criterion*1		Unit	Remarks
		Lower Limit	Upper Limit		
Electrical characteristics	Voltage gain	$L - 3$	$U + 3$	dB	
	Rated output	$L \times 0.9$	—	W	
	Total harmonic distortion	—	$U \times 1.5$	%	
	Output noise voltage	—	$U \times 1.5$	V	Including pulse noise
	Input limiting voltage	—	$U + 3$	dB μ	
	Current drain	—	$U \times 1.1$	A	
	Input offset voltage	—	$U \times 1.5$	V	
	Input offset current	—	$U \times 1.5$	A	
	Input current, input bias current	—	$U \times 1.3$	A	
	Maximum output voltage amplitude	$L \times 1.1$	$U \times 0.9$	V	
	Common mode input voltage range	$L \times 0.9$	—	V	
	Common mode discrimination ratio	$L - 3$	—	dB	
	Slew rate	$L \times 0.9$	—	V/ μ s	
	Open and short circuit	Open circuit, semi-open circuit, short circuit, semi-short circuit	Also includes high and low temperature failures	—	
Appearance and other aspects	Appearance	According to the limit samples		—	
	Corrosion/discoloration	According to the limit samples		—	
	Solderability	According to the limit samples		—	
	Marking	According to the limit samples		—	

Note: 1. U: Upper limit value for the initial ratings
L: Lower limit value for the initial ratings

1.2 Reliability Test Results

Table 2 lists the reliability test results for linear ICs for use in information industry applications.

This table collects the test results for operational amplifiers, comparators, and voltage regulators.

Table 2 Reliability Test Results for Linear ICs for the Information Industry

Test Item	Plastic Seal				Test Conditions
	No. of Tests	Total Test Time	No. of Failures	Failure Rate (1/hr)* ¹	
High-temperature operation	9.552	9,082,000	5	5.5×10^{-7}	Ta = 125°C V _{CC} = V _{CCMax} (V _{EE} = V _{EEMax})
High-temperature storage	829	793,000	0	1.2×10^{-6}	Ta = 150°C
Low-temperature storage	509	509,000	0	1.8×10^{-6}	Ta = -55°C
High-temperature high-humidity storage	3.110	2,727,000	0	3.4×10^{-7}	Ta = 65°C, 95%RH Ta = 85°C, 85%RH V _{CC} = V _{CCMax} (V _{EE} = V _{EEMax})
High-temperature high-humidity operation	443	44,000	0	2.1×10^{-6}	
Thermal cycle	117.210	—	0	—	-55°C to +150°C, 10 cycles
Thermal cycle life	13.630	—	2	—	-55°C to +150°C, 200 cycles
Thermal shock	398	—	0	—	0°C to 100°C, 10 cycles
Soldering thermal stress resistance	404	—	0	—	260°C, 10 s
Drop test	160	—	0	—	1500G, 0.5 ms, X, Y, and Z directions, 3 times each
Vibration	160	—	0	—	60 Hz, 20G, X, Y, and Z directions, 32 h
Variable frequency vibration	160	—	0	—	100 to 2,000 Hz, 20G, X, Y, and Z directions, 3 times each
Fixed acceleration	160	—	0	—	20,000G, X, Y, and Z directions, one minute each
PCT	360	—	0	—	Ta = 121°C, 2 atmospheres, 60 h
Solderability	160	—	0	—	230°C, 5 s, rosin-based flux
Pin strength	90	—	0	—	225g, 90° bend, 3 cycles

Note: 1. Reliability level: 60%

2. Usage Notes

Semiconductor device reliability is not due solely to factors inherent to the device. Reliability is also influenced by the usage conditions, that is the circuit conditions, environmental conditions, and other conditions determined by the user. This section describes points requiring special care that should be kept in mind during system design and during handling and storage so that Renesas semiconductor products may be used at even higher reliability levels. This section also presents specific examples to illustrate these points.

First, this section discusses ratings and device package aspects that should be taken into consideration during device selection, and additionally presents points that require care in circuit design and with respect to ESD (electrostatic discharge). Then, along with listing the points that require care when mounting devices, a separate section is dedicated to notes on surface mounting products. After presenting notes on packing and transporting semiconductor devices, this section concludes with notes on product safety.

2.1 Notes on Device Selection

This section presents points that we would like our customers to keep in mind when selecting devices. In particular, this section discusses the maximum ratings, derating, and package selection.

2.1.1 Maximum Ratings

The maximum ratings for semiconductor devices are normally stipulated as "Absolute Maximum Ratings". The values specified in the maximum rating tables for each product are values that must not be exceeded, even momentarily. The Japanese Industrial Standard JIS C 7032 defines these ratings as follows:

"Absolute maximum ratings: Limit values that must not be exceeded even momentarily. When rating values are specified for two or more items, these are limit values such that no two items are allowed to reach their rated value at the same time." (From JIS C 7032)

Degradation or destruction is possible when a rated value is exceeded even momentarily. Furthermore, even if the device continues to operate after that event, the life of the device may be shortened radically. Therefore, when designing electronic circuits that use semiconductor devices, the designer must assure that the maximum ratings specified for the device are not exceeded, whatever changes in external conditions occur during device use. A related point is that the items specified in the maximum ratings are often intimately and mutually related. Thus special care is required so that these values are never reached at the same time. For example, even if the current and voltage applied to a transistor always remain under their maximum ratings, since the power is given by the product of those values, care must be taken that this product remains within the allowable collector loss for the transistor. Also remember that in addition to DC maximum ratings, the safe operating range (ASO), the load locus, and the peak voltage and current require attention in applications with pulse characteristics.

2.1.2 Notes on Circuit Design

From the standpoint of reliability design, while fulfilling the initial characteristics in the circuit design goes without saying, adequate margins must be provided in the design by applying derating and taking characteristics variations into account. The following points should be seen as problems from the standpoint of reliability: wiring problems, external surges, reactive loads, noise margin, the safe operating range (ASO), reverse bias, flyback pulses, ESD, pulse stress, high electric fields, and latchup.

2.2 General Points

2.2.1 Preventing Noise and Surge Voltages

The problems of surge voltages, static electricity, and noise are common to all semiconductor devices, and measures must be taken to remove the sources of these phenomenon and to reduce their magnitude.

In general, electronic equipment is usually designed assuming that fluctuations in the commercial power system will be about $\pm 10\%$. However, if equipment that generates surge voltages is installed in the vicinity, breakdowns and incorrect operation may occur due to variation in the power system voltage. Such problems are usually due to overlapping surges in the power lines, but pulse-type surges can also be induced in power lines by lighting or other phenomenon. These problems can be ameliorated by inserting a filter such as the one shown in figure 1 in the AC side of the power line. Shielding or some other measure is required in cases where even though surge and static do not enter the circuit indirectly from the AC power line, it is possible for extraneous voltages to be directly applied to components or semiconductor devices on the circuit board. Note that it is critical that the shield have a low impedance to ground. The shielding may not be effective if this impedance is too high.

Protection circuits are sometimes inserted in circuits where it is possible for static electricity or surge pulses to be applied as noise. Figure 2 shows a special case of such a circuit. Here the time constant defined by $R_1 \times C_1$ must be set up to be in a range that does not influence circuit operation yet is still effective at absorbing surge pulses and other noise.

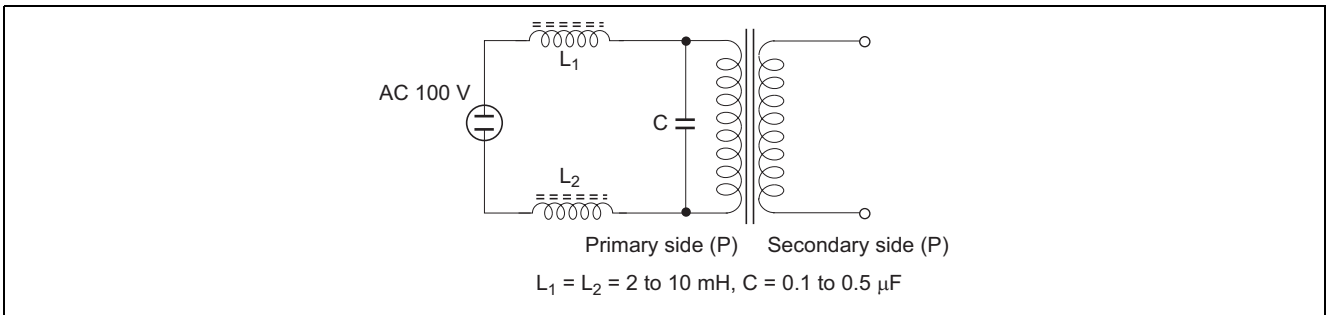


Figure 1 Sample Surge Suppressing Circuit

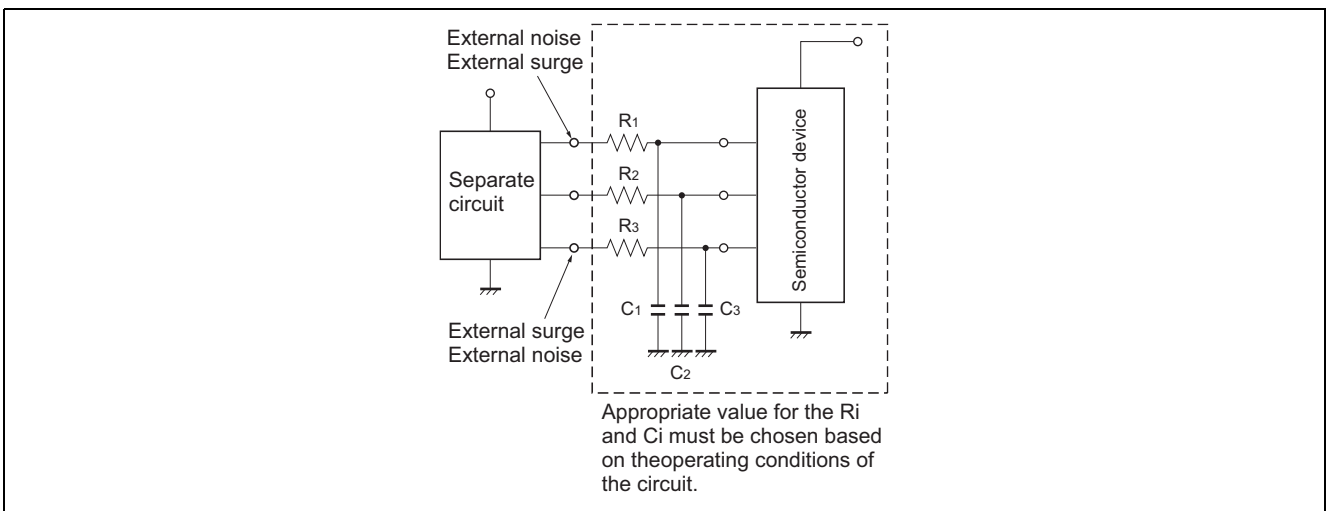


Figure 2 Sample Surge Protection Circuit

(1) Noise Types

There are two types of noise that cause problems in mounted circuits: noise that occurs between ground and signal lines, and noise that is induced between signal lines (see figure 3). The influence on device operation and the measures used to reduce these noise types differ.

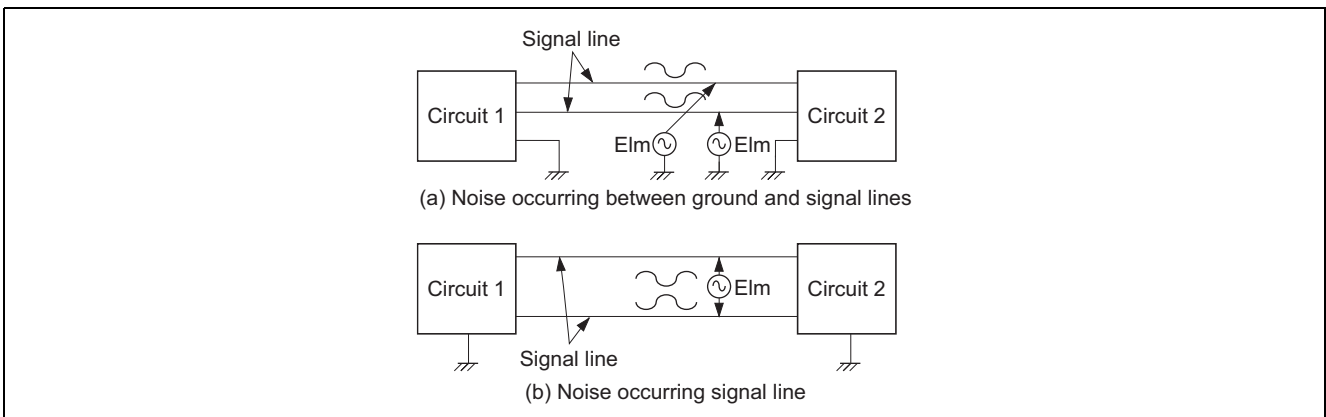


Figure 3 Noise Types

(2) Noise Source to Signal Line Coupling

There are several types of coupling between noise sources and signal lines. The following items list several examples.

— Coupling due to conduction

A leakage impedance exists between the noise source and the signal line.

— Capacitive coupling

Capacitive coupling exists between the noise line and the signal line.

— Electromagnetic induction

A mutual conductance exists between two signal lines.

— Crosstalk

If two or more lines are run adjacent to each other, a noise voltage may be induced in one line by signals in the other due to capacitive coupling or electromagnetic induction.

— Ground loops

When a signal line is grounded at both the transmitting and receiving sides, the potential difference between the two grounds may appear as noise.

— Reflections

Reflected waves due to impedance mismatches in signal lines can overlap the signal and appear as noise.

Figure 4 shows these schematically.

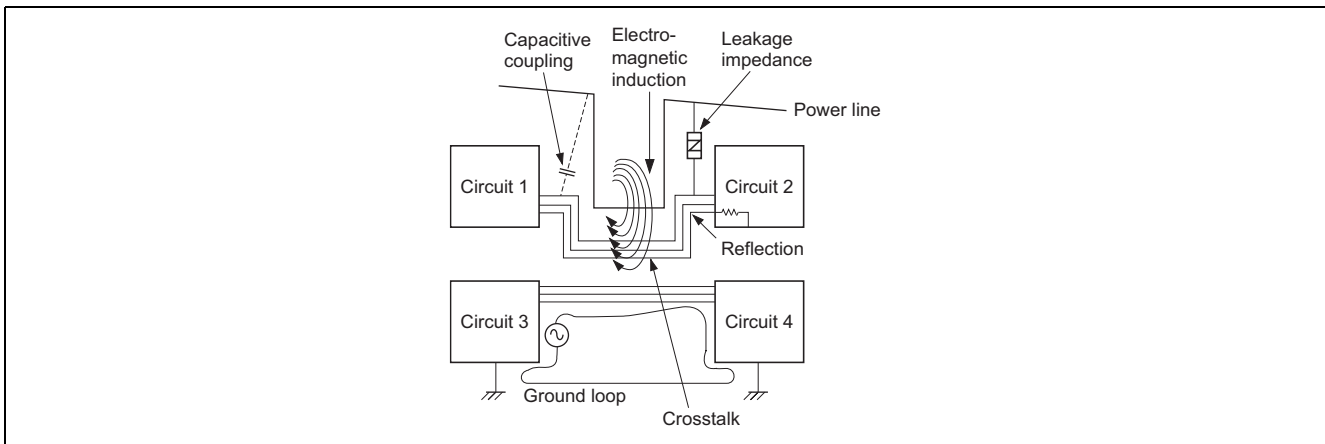


Figure 4 Noise Source to Signal Line Coupling

(3) Noise Exclusion Techniques

To create a system in which noise is not a problem, the designer must take measures such as discovering and removing noise sources, designing the circuit with large noise margins so that it cannot pick up noise, and providing correction circuits.

— Noise source countermeasures

When possible, the most effective technique for reducing noise is to deal with the noise source. These techniques include reducing surge voltages by inserting diodes in parallel with relay coils or inserting resistor-capacitor circuits and inserting filters in the noise source side of power lines for noise that enters a circuit from the AC line. Also note that when equipment that generates strong electric fields is the noise source, the needs for noise reduction measures in the system receiving the noise can be reduced by applying techniques such as shielding at the noise source. Also, steps such as separating the noise source from the affected circuit should be considered.

Since electromagnetic noise generated by equipment is the object of radio frequency interference regulations, system designers must consider generated noise as well as received noise.

— Ground line countermeasures

Circuit system interference due to current flowing in the ground system can be removed by providing a dedicated ground line for the circuit system and completely isolating that ground line from ground systems such as other power supply lines. Also, the circuit system and the equipment case should be connected only at a single point so that no loops that include both the circuit system and the case are formed (see figure 5).

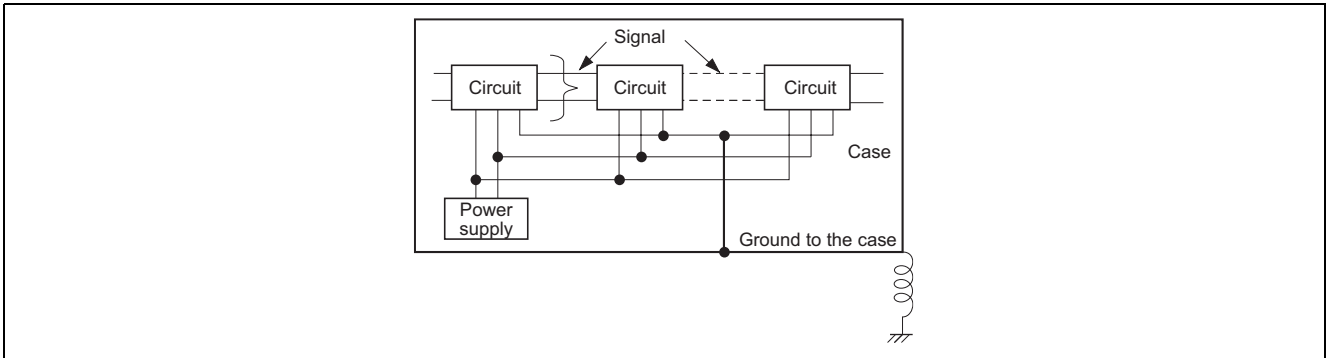


Figure 5 Circuit System Grounding

— Countermeasures based on shielding

Shielding the whole signal line system is a good technique for reducing the influence of external noise. For capacitive coupling noise, wrap the signal line system with a good conductor and ground that conductor. This causes the currents that would have been induced in the signal lines if there were no shield to be induced in the shield and shunted to ground. If the system is operating in the presence of strong magnetic fields, cover the signal line system with a magnetic material to reduce the magnetic field in the signal line system (see figure 6). Usually, steel pipe is used, since materials with a high magnetic permeability are costly. Factors such as the noise level, costs, and increasing the mechanical strength of the signal line system must be taken into account when determining the shielding technique to be used.

Another shielding technique that is often used is the twisted pair. Noise can be reduced if a 2-line signal line is made symmetrical as seen from the signal source, the receiving circuit, ground, and noise sources. External noise can be reduced if the twist pitch of the signal line is made tight relative to the transmission distance. Furthermore, noise due to electromagnetic induction can be reduced by also shielding the twisted pair. In case of the twisted pair, there is possibility that ground loop occurs. However, ground loop can be removed by doing as figure 7.

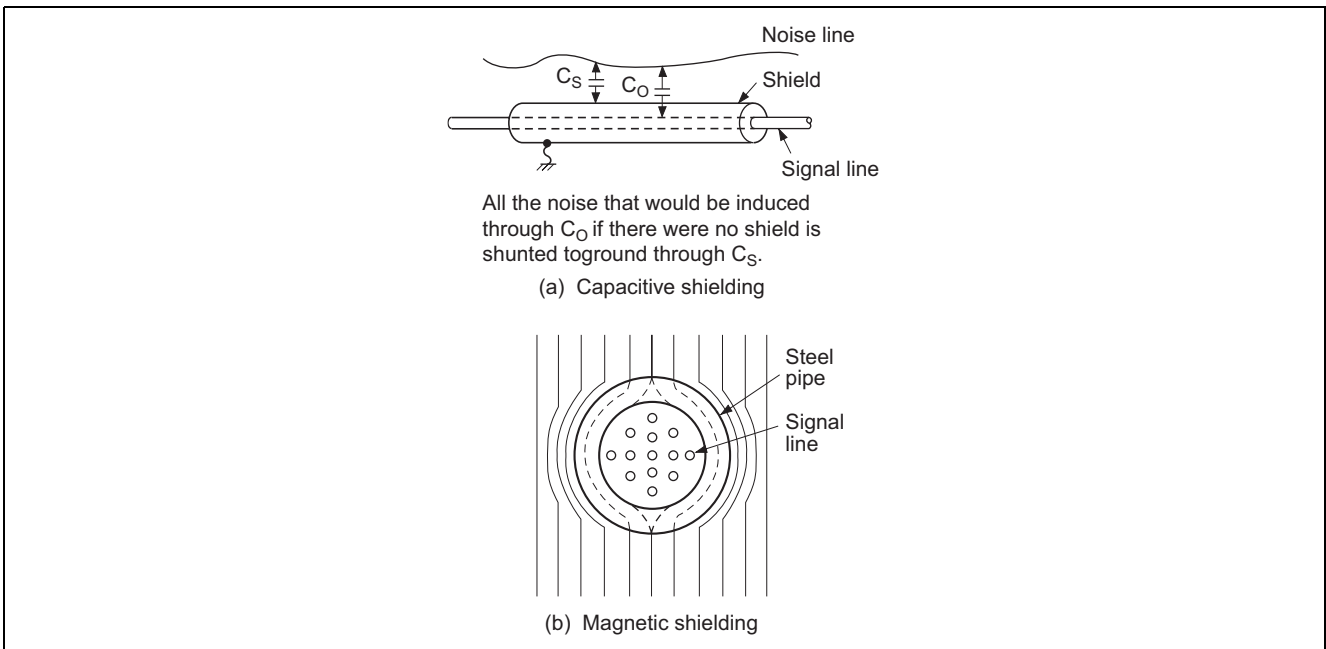


Figure 6 Shielding Techniques

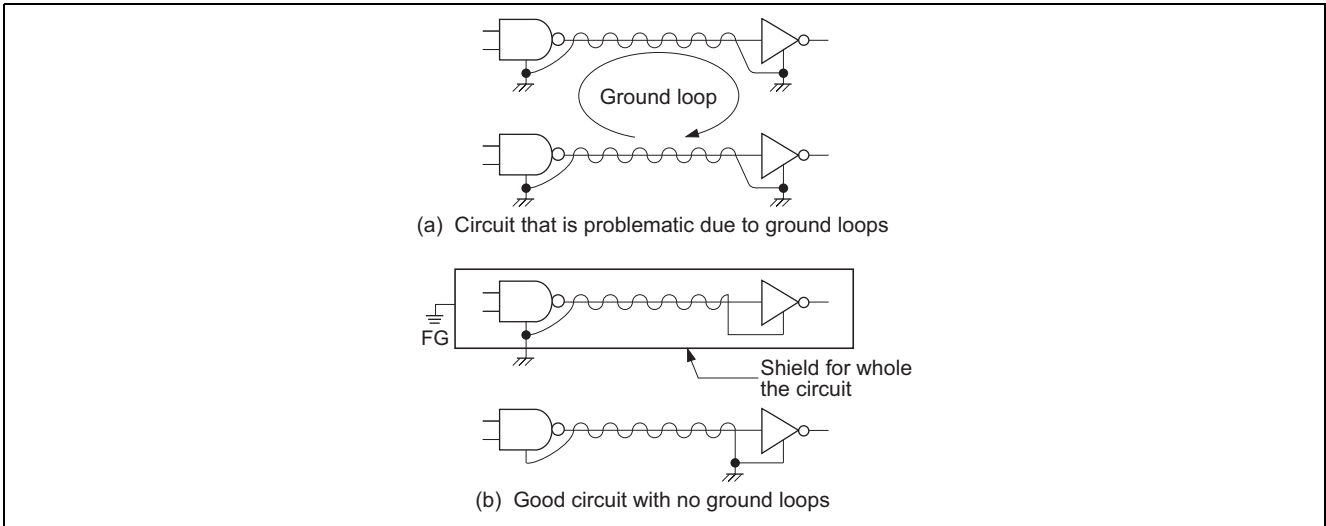


Figure 7 Wiring Types Using Twisted Pairs

— Countermeasures based on filters

Since in general, noise in power supply systems often enters from the AC line, an AC line filter should be inserted at the source of the noise or in the AC supply side of the circuit system. Also, the power supply impedance as seen from the circuit system must be lowered as much as possible. Lower the impedance with respect to noise by inserting capacitors at each critical point in the power supply lines. Here, it is desirable to insert large capacitors in parallel as a relatively low frequency bypass.

(4) Surge Countermeasures

Circuit systems are often placed in environments where surge voltages may be applied. This section describes the major problems of this type.

When an IC is used in the vicinity of a high-voltage circuit, such as in applications that include a CRT in the same case, surge voltages may be applied due to discharges. Figure 8 and 9 show examples where resistors, capacitors, and other components are inserted at the IC pins to absorb and suppress surge voltages. The degree to which these surge voltages can be reduced is seen as a major factor for improving IC reliability. Figure 8 shows an example in which a resistor and a capacitor are inserted as an IC output stage protection circuit to reduce surges induced in the IC leads. Figure 9 shows an example in which surges entering from the power supply are absorbed. This example is appropriate as a countermeasure for surges due to ignition noise in automotive systems. Circuit designers must search for the paths over which surges enter circuits and the pins at which surges enter the ICs and apply the countermeasures described here to prevent the destruction of semiconductor devices due to surge voltages.

A problem that is easy to overlook is incorrect circuit operation or even semiconductor device destruction due to potential differences due to surges that arise between power lines that were originally thought to be at the same potential (see figure 10). In the original design, points A and B (or points A' and B') were at the same potential. However, due to the impedance between A and B, a surge can result in a potential difference between these points. Possible countermeasures for this type of problem include using wiring or a wiring scheme in which induction due to surges does not occur, installing shielding, and re-analyzing the system grounding.

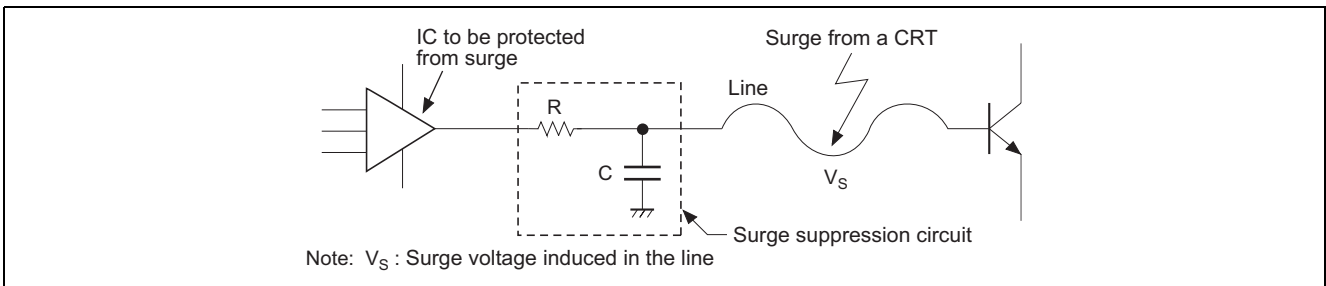


Figure 8 Sample RC Surge Protection Circuit

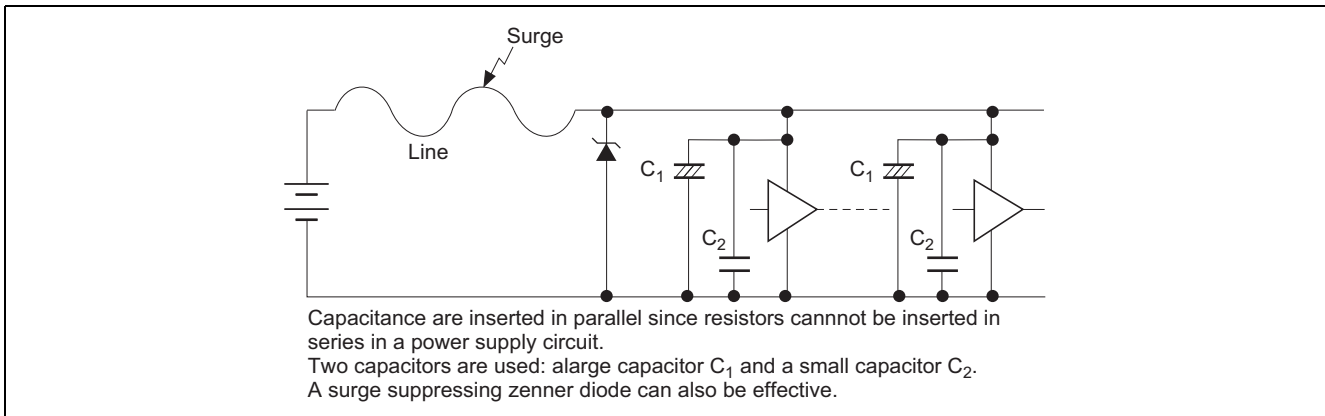


Figure 9 Power Supply Line Surge Suppression Example

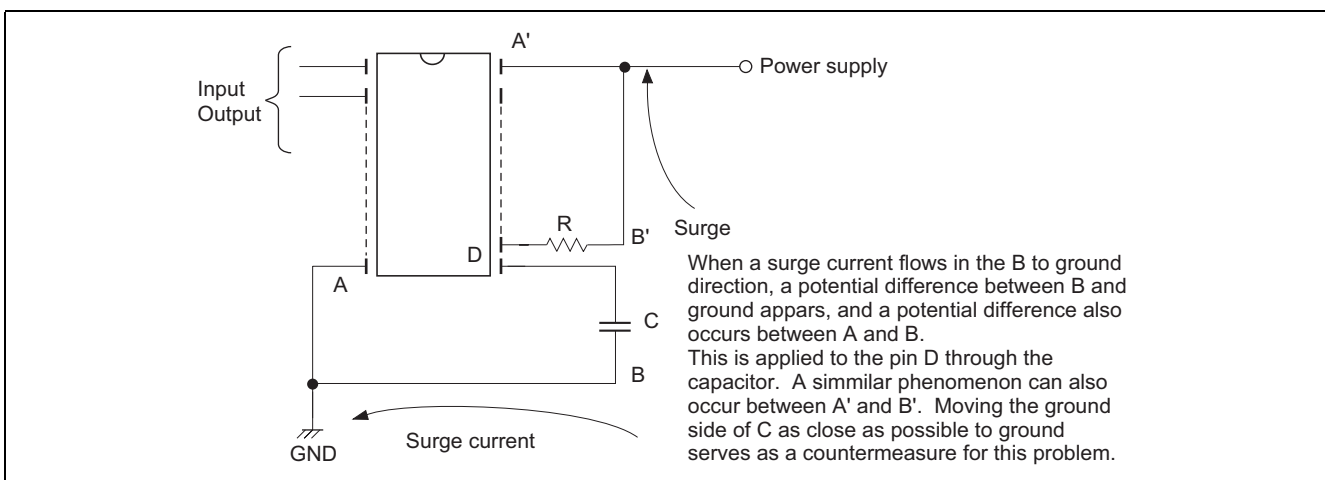


Figure 10 Surge Suppression Measures in Power Supply Lines

(5) Influence of High Electric Fields

The application of a strong electric field for extended periods can polarize and charge the device's package itself. This can change the device's threshold levels and degrade its characteristics in general.

If the device is removed from the circuit and the LSI is tested independently, the degraded characteristics may recover naturally, since the strong electric field has been removed. This can result in irreproducible errors. High fields should either be avoided or else LSIs should be shielded to prevent charging.

(6) Handling Unused Pins

Incorrect operation due to crosstalk from other circuits can occur if unused input pins are left open. Unused input pins should be connected to ground through an appropriate impedance or else connected to the power supply line. Do not use NC pins as signal connection points when designing circuit boards. Some NC pins in some LSI products are actually connected to LSI pads and incorrect operation or even damage to the LSI can occur if voltages are applied. These pins should be connected to a common power supply or ground line, or left open.

(7) Latchup

This phenomenon occurs due to unexpected surges that exceed the maximum ratings, ripple in the power supply, or noise or regulation problems. It can also occur due to differences in power supply rise times in devices that operate with two power supplies. These problems may also lead to destruction of the device itself. Thus latchup prevention must be adequately considered during system design.

(8) Oscillator Circuits

When using products that include built-in oscillator circuits, be sure to use external components that have characteristics that fall within the recommended ranges stipulated individually. Also note that an oscillator circuit may not function correctly if other signal lines pass nearby as shown in figure 11. Avoid this sort of wiring when designing circuit boards, and locate crystal oscillators and capacitors as close as possible to the oscillator pins. Figure 12 shows a specific example of board design.

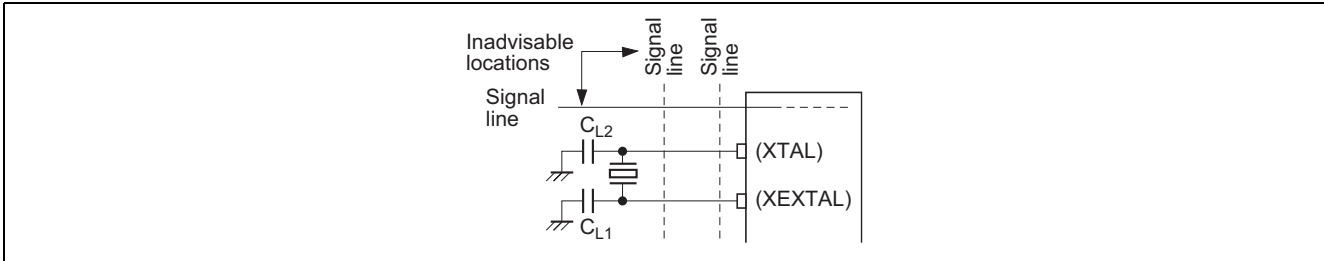


Figure 11 Inadvisable Crystal Oscillator Connections

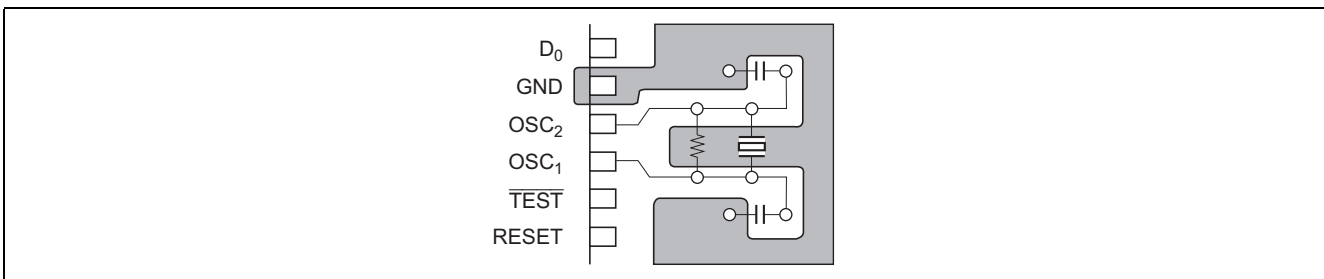


Figure 12 Sample Board Design

2.2.2 General Notes on Electrostatic Discharge (ESD)

(1) Work Environment

Static charges accumulate more easily as the relative humidity decreases. Although surface mounting devices must be stored in a dry atmosphere to prevent moisture absorption, from the standpoint of preventing static buildups, it is important to maintain the relative humidity in the 45 to 75% range during handling and during the process of mounting devices on circuit boards.

(2) Operations

The use of insulating materials and objects (in particular synthetic fibers and plastic products) that are easily charged should be avoided as much as possible in the work place, and conductive materials should be used in their place. Antistatic clothing and ionized air blowers are examples of recommended antistatic measures.

When handling semiconductor devices, attempts should be made to store and transport devices only in containers made from conductive materials or materials that have received some sort of antistatic processing, for example static shielding bags and conductive mats.

— Equipment and facilities

Test and measurement equipment, conveyors, work tables, floor mats, jigs, solder baths, and soldering irons must be thoroughly grounded so that static charges cannot accumulate. Conductive mats (10^6 to $10^{11} \Omega$) should be placed on work stands and the floor and grounded individually.

— Personnel

Personnel must be grounded during work. However, to prevent shocks, ground personnel through a series resistor of at least 1 M Ω .

Also, personnel should not touch devices with their bare hands, but should wear gloves. Fabrics that easily accumulate static charges, such as nylon, must not be used. While a resistance of between 1 M Ω and 100 M Ω is considered appropriate for shoes and sandals, note that this resistance may change due to dirt, wear, humidity, and other factors.

— Procedures

Use soldering irons specifically designed for use with semiconductor devices (such soldering irons operate at 12 V to 24 V), and ground the tip. When handling devices, handle each device as few times as possible, and complete operations quickly. These two points are often the key to preventing device destruction during assembly.

2.3 Notes on Handling Surface Mounting Devices

This section presents a concrete discussion of handling and mounting conditions for surface mounting devices, a device type that has seen a rapidly increasing popularity in recent years.

2.3.1 Notes on Handling

Surface mounting devices require solder processing from the side of the device that is mounted on the printed circuit board, and have a structure that can be said to be truly susceptible to thermal stress during mounting. In particular, when mounting techniques that heat the whole package are used, the following points must be kept in mind during that process. Refer to the "Surface Mounting Package Mounting Manual" published by Renesas Technology Corp. for more details.

(1) Package Moisture Absorption

Moisture absorption is unavoidable in the epoxy resins used for plastic packages if the packages are stored in a high relative humidity. If the amount of moisture absorbed becomes significant, that moisture may vaporize abruptly during solder mounting and separate the resin from the lead frame. In severe cases, this phenomenon may even crack the package. Thus storing surface mounting package devices in a dry atmosphere is extremely important. Moisture-proof packing is used to prevent moisture absorption for products that require moisture absorption management.

These products should be stored under the following environmental conditions after opening the moisture-proof packing to prevent any further moisture absorption. Furthermore, we strongly recommend that reflow soldering be performed within one week of opening the moisture-proof packing.

Temperature : 5 to 30°C

Relative humidity : 60%RH, or lower

When returning products to storage after opening, insert silica gel packets that have not absorbed moisture (the blue indicator should be clearly visible) in the packing, reseal the packing, and store under the above environmental conditions.

We recommend baking products that are suspected of absorbing moisture for 16 to 24 hours at 125°C to remove any moisture that was absorbed during transportation, storage, or handling.

(2) Improving Moisture Resistance

Since the molded resin is thinner and the distance from the external leads to the internal IC chip is shorter for surface mounting products than conventional plastic-sealed DIP products, moisture resistance may require special consideration in some cases. For example, measures such as resin coating may be required for outdoor equipment or equipment in which moisture resistance is particularly important. While polyurethane, silicone, and other resins are used as coating materials, note that hardening and contraction stress and the stress due to the difference in thermal expansion coefficients between the resin and the circuit board can crack the device, crack the solder joint between the lead and the board, or cause open circuits. Thus adequate care is required in selecting the coating material and determining the structure of the coating.

2.3.2 Recommended Process Conditions for Different Mounting Methods

The most common mounting methods used for surface mounting devices are the IR reflow method and the vapor phase reflow method (Do not use the solder dip method). Since these mounting methods all heat the whole package, they all apply strong thermal stresses to the device. Thus, from the standpoint of maintaining reliability, the temperature of the package surface, as well as the temperature of the solder joint, must be managed carefully. Accordingly, the package surface temperature is specified in the recommended mounting process conditions for Renesas products.

Next we describe the ideas behind the recommended process conditions referring to figure 13.

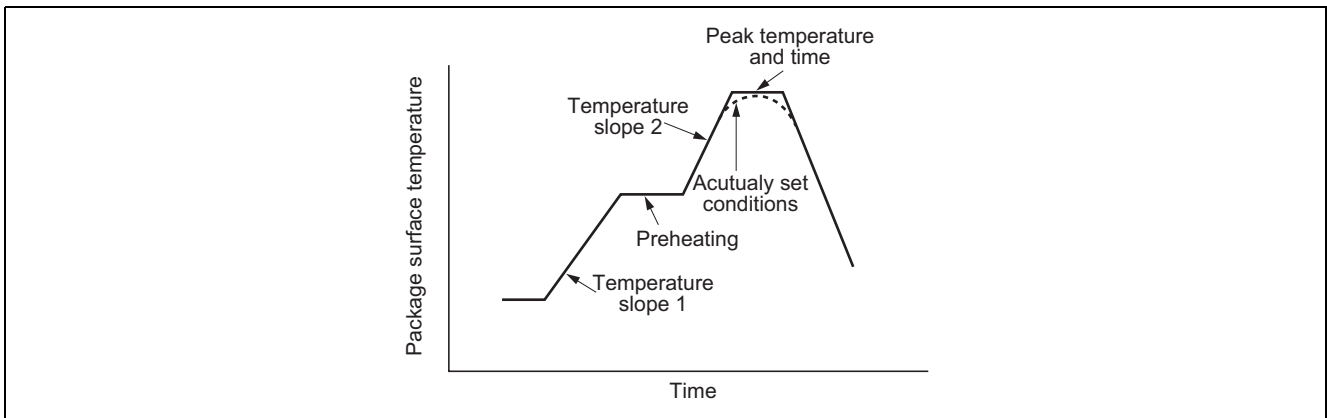


Figure 13 Recommended Process Conditions

(1) Temperature Slope 1

If the temperature were raised rapidly, the temperature of the various parts of the package (e.g., the front, inside, and rear) would become unequal. The resultant differences in expansion due to the thermal expansion coefficient could cause the package to warp and damage the chip. Therefore, the upper limit on the rate of temperature increase must be observed carefully. The lower limit is determined by the operating efficiency of the reflow unit.

(2) Preheating

This period is provided to bring all components and the printed circuit board to the same temperature at a temperature just below the melting point of the solder, to stabilize the solder joint, and to lessen thermal shock. In general, this temperature is set in the vicinity of the rated temperature for the surface mounting device.

(3) Temperature Slope 2

The upper limit for this temperature increase rate is the same as that for slope (1), and the lower limit is determined by the necessity of holding the peak temperature and time discussed in item (4) below within the stipulated limits.

(4) Peak Temperature and Time

These parameters require the utmost care to hold the damage to the package to the absolute minimum. Since the peak temperature degrades the package strength (according to the temperature characteristics of the resin used) and directly influences the water vapor pressure within the package, a peak temperature as low as possible is desired. Also, since the water vapor pressure increases with time, the time must be kept as short as possible. The process conditions specified by Renesas correspond to the intersection of the allowable ranges discussed above and the ranges where it is possible to actually form a solder joint. However, since these are specified not as average values but as upper limits, care must be taken not to exceed these limits when setting the process conditions (for example, see the dotted line in figure 13).

Figure 14 shows the Renesas recommended process conditions for IR reflow.

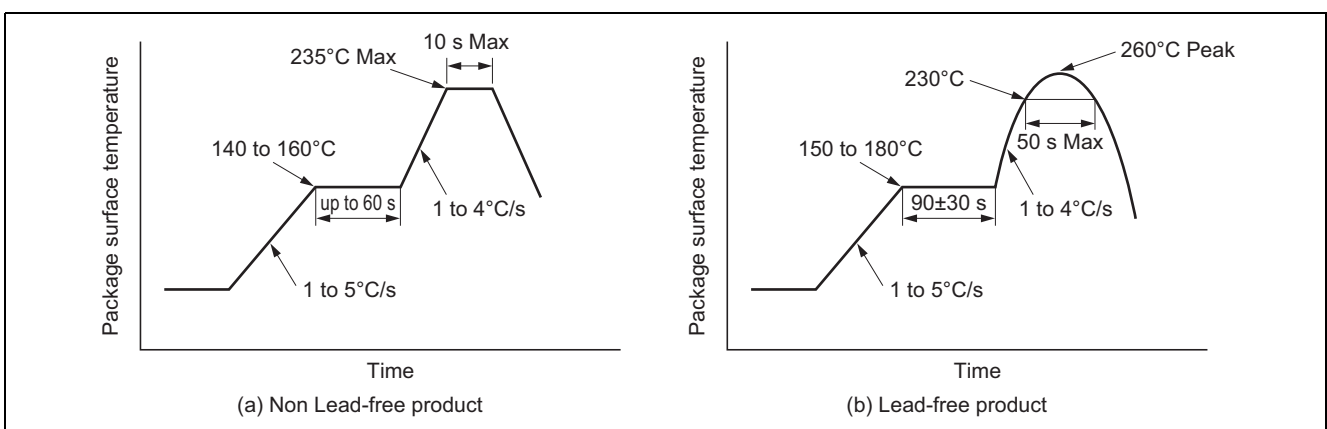


Figure 14 Recommended Process Conditions for IR Reflow

2.4 Other Notes

2.4.1 Notes on Chemical Reactions

Materials with a significant sulfur content, such as rubber, may emit sulfur gas. If such materials are placed near an IC and condensation occurs due to high humidity, chemical reactions may occur in between the IC leads. The foreign substances thus formed may result in current leakage. Since it is also possible for chemicals other than sulfur to react chemically with an IC's structural components, this possibility should be taken into consideration when designing products that incorporate ICs.

2.4.2 Notes on SOP Package Usage

(1) Derating

- Apply the individual IC specifications for P_T for each IC.
- The allowable temperature T_j (Max) for an IC's junctions is given by the following formula for the general case.

$$T_j (\text{Max}) = \theta_{j-a} \cdot P_c (\text{Max}) + T_a$$

(Here, θ_{j-a} is the thermal resistance when mounted on a board, and P_c (Max) is the IC's maximum allowable power dissipation.)

Therefore, the board wiring density and the board material must be selected to match the effective board thermal conductivity so that T_j (Max) does not exceed 125°C for the P_c (Max) value during circuit operation. Note that care must be taken so that P_c (Max) does not exceed P_T .

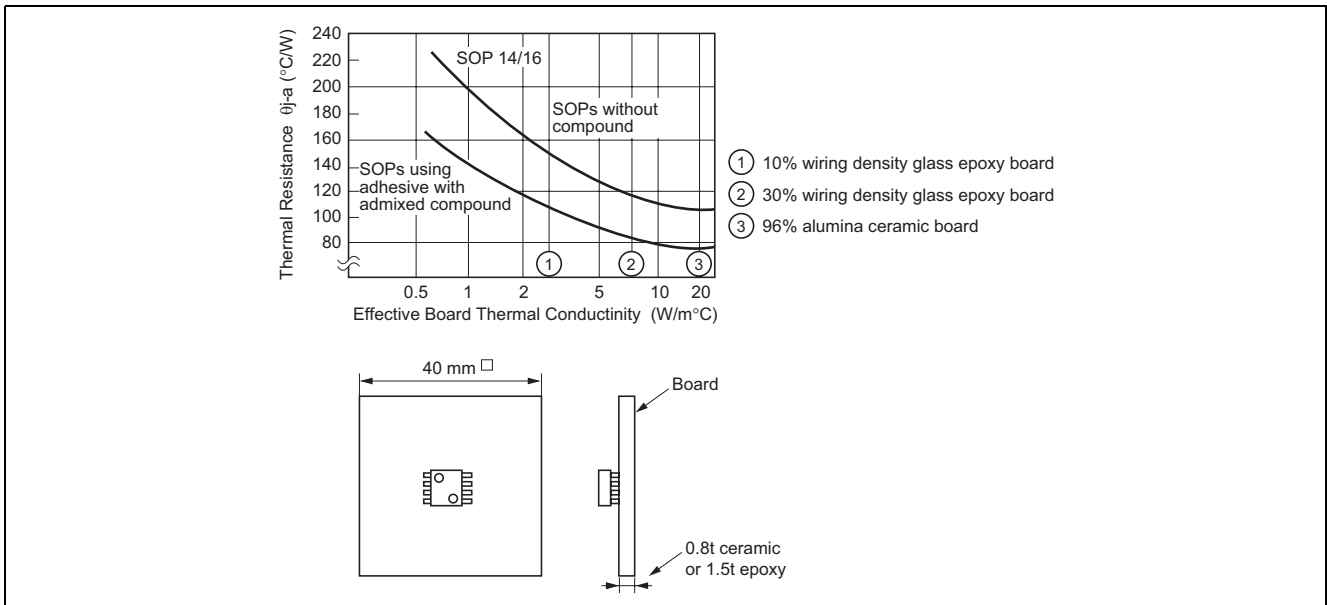


Figure 15 SOP Thermal Resistance

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.28.04	—	First edition issued

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors. Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.