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# H8S/2200 Series

## Data Transfer in the Single-Address Mode

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### Introduction

Uses the DMAC single-address mode to transfer data to an external device (H8S/2215). DMAC is started up at a falling edge of an external signal.

### Target Device

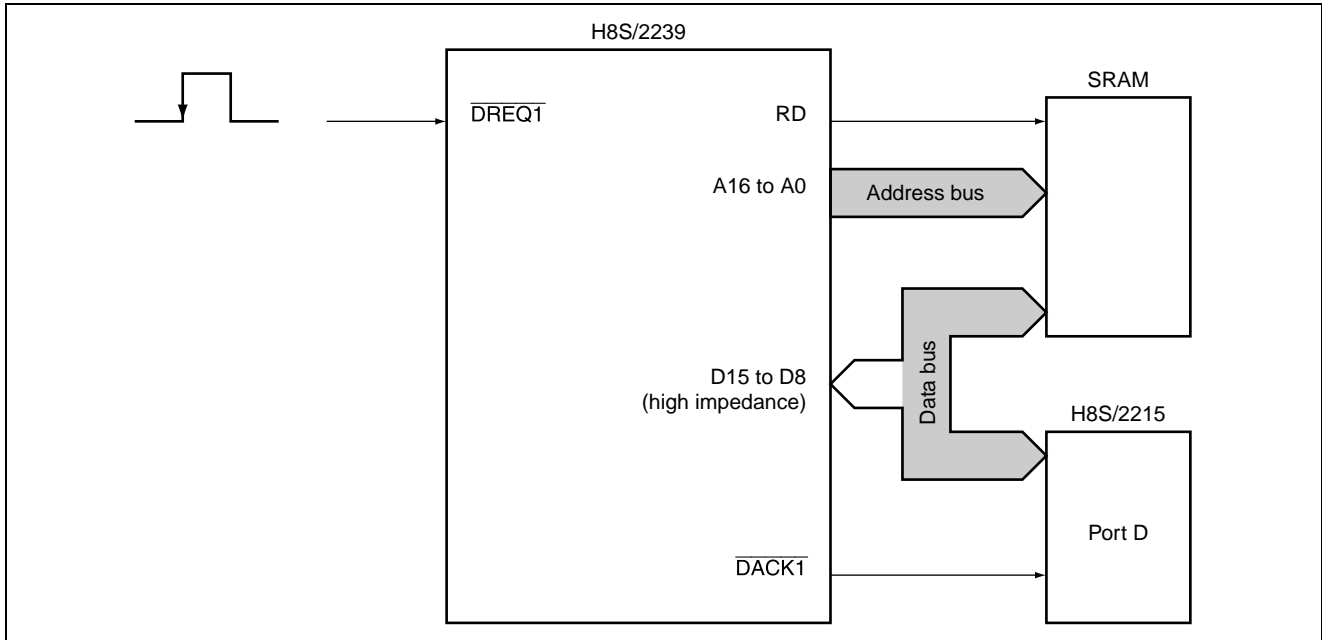
H8S/2239

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**1. Specifications**

1. As shown in figure 1, this sample task uses DMAC single-address mode to transfer data between the external space specified by a transfer source address or transfer destination address, and an external device that is selected by a DACK strobe independently of the address.
2. DMAC starts up at detection of a falling edge of an external signal.



**Figure 1 Data Bus in the Single-Address Mode**

## 2. Description of Functions

1. This sample task uses the DMAC single-address mode (idle mode specification) to transfer data to the external device (H8S/2215) from the external memory (SRAM).

A. The block diagram of DMAC to be used in this sample task is shown in figure 2.

This sample task uses the following DMAC functions to transfer data blocks:

- Function that starts up DMAC on an external request (DMAC startup by DREQ)
- Function that transfers one byte or one word between the external memory and external device per transfer request as many times as specified (single-address mode)

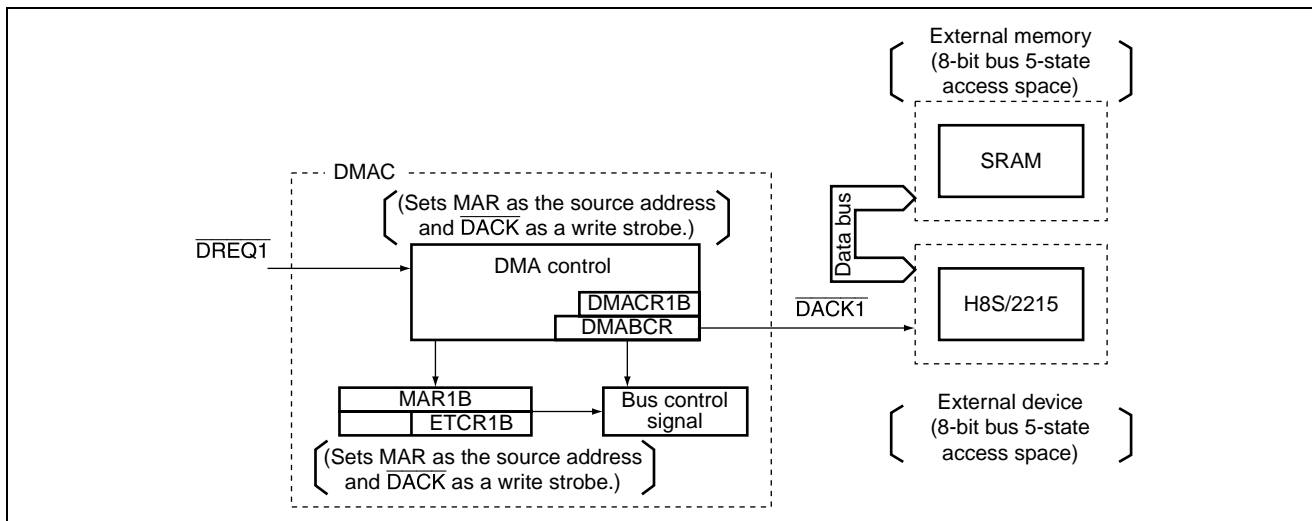


Figure 2 Block Diagram of DMA Controller

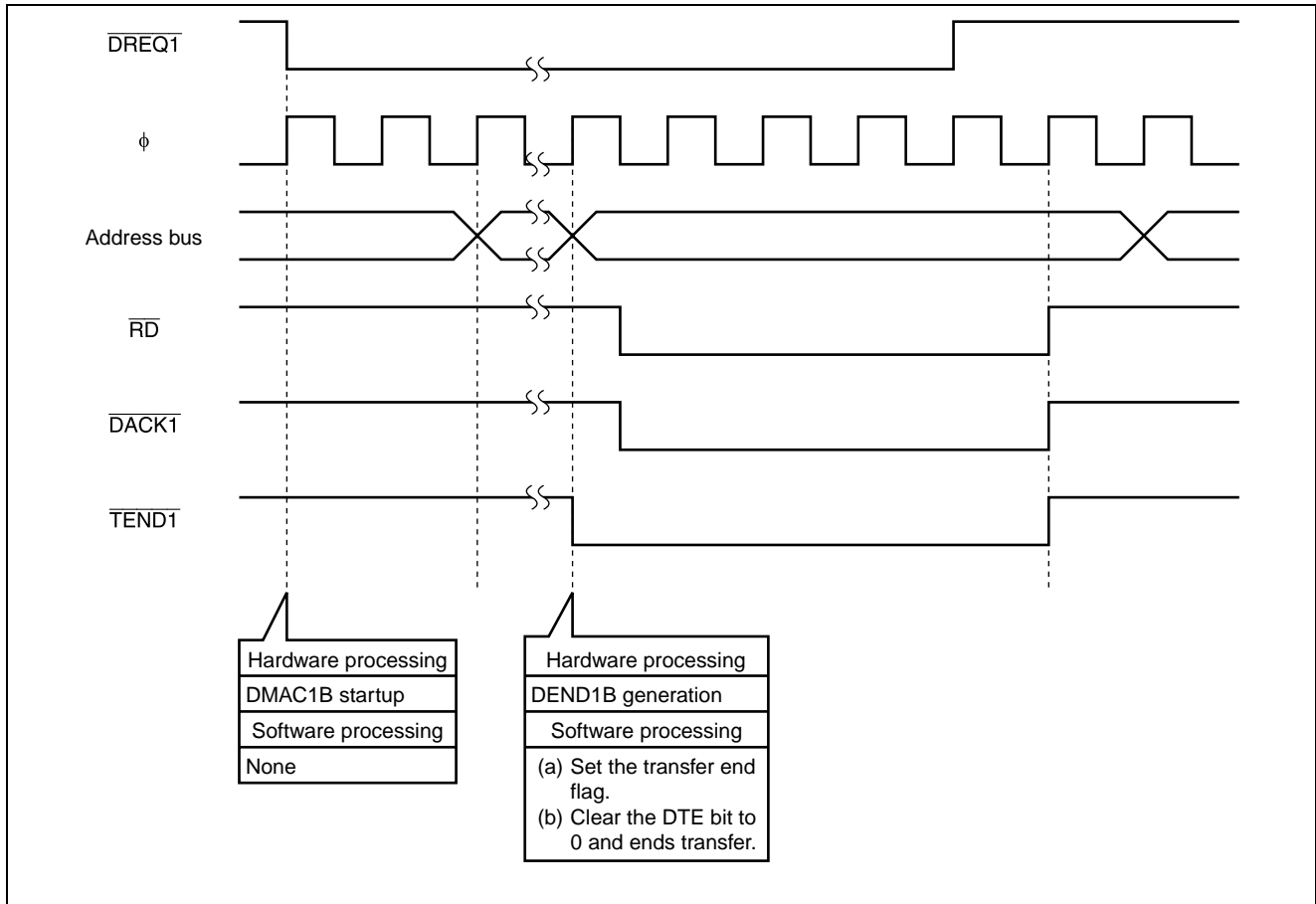
2. Function allocation of this sample task is shown in table 1. This sample task allocates the H8S/2239 functions as shown in table 1 to transfer blocks.

Table 1 Assignment of Functions

Elements	Description
DREQ1	Inputs an external pulse that functions as a trigger for DMAC startup.
DACK1	Data transfer acknowledge
DMABCR	Controls operation of each channel.
DMACR1B	Sets DMAC in the idle mode.
MAR1B	Sets the transfer source address.
ETCR1B	Sets a transfer count.

**3. Principles of Operation**

The principles of operations used are shown in figure 3. This sample task performs H8S/2239 hardware processing and software processing as shown in figure 3 to transfer one byte to the 8-bit 5-state access space in the external device from the external 8-bit 5-state access space.



**Figure 3 Principles of Operations Used of Transfer in the Single-Address Mode (Byte Read)**

## 4. Description of Software

### 1. Description of Modules

Module Name	Label Name	Function
Main routine	singlemn	Performs initial setting of DMAC.
Data transfer end	transend	Sets the transfer end flag.

### 2. Description of Arguments

Elements	Function	Data Length	Used in	I/O
status	Flag indicating data transfer end	unsigned char	Main routine	Input
	1: Transfer ended 0: Transfer in progress		Transfer end	Output

### 3. Description of Internal Registers Used

Register Name	Function	Used in
DMABCRH	Sets DMAC1B in the single-address mode of the short-address mode.	Main routine
DMABCRL	Enables data transfer.	Main routine
DMACR1B	Sets DMACR as follows: <ul style="list-style-type: none"> <li>• Byte size transfer</li> <li>• Idle mode</li> <li>• Increment MAR after data transfer</li> <li>• Data transfer direction (MAR is set as the source address and the DACK pin as a write strobe.)</li> <li>• Falling edge of the DREQ signal is set as the startup source.</li> </ul>	Main routine
MAR1B	Sets the transfer source address.	Main routine
ETCR	Sets a transfer count.	Main routine
MSTPCR	Cancels DMAC module stop mode.	Main routine

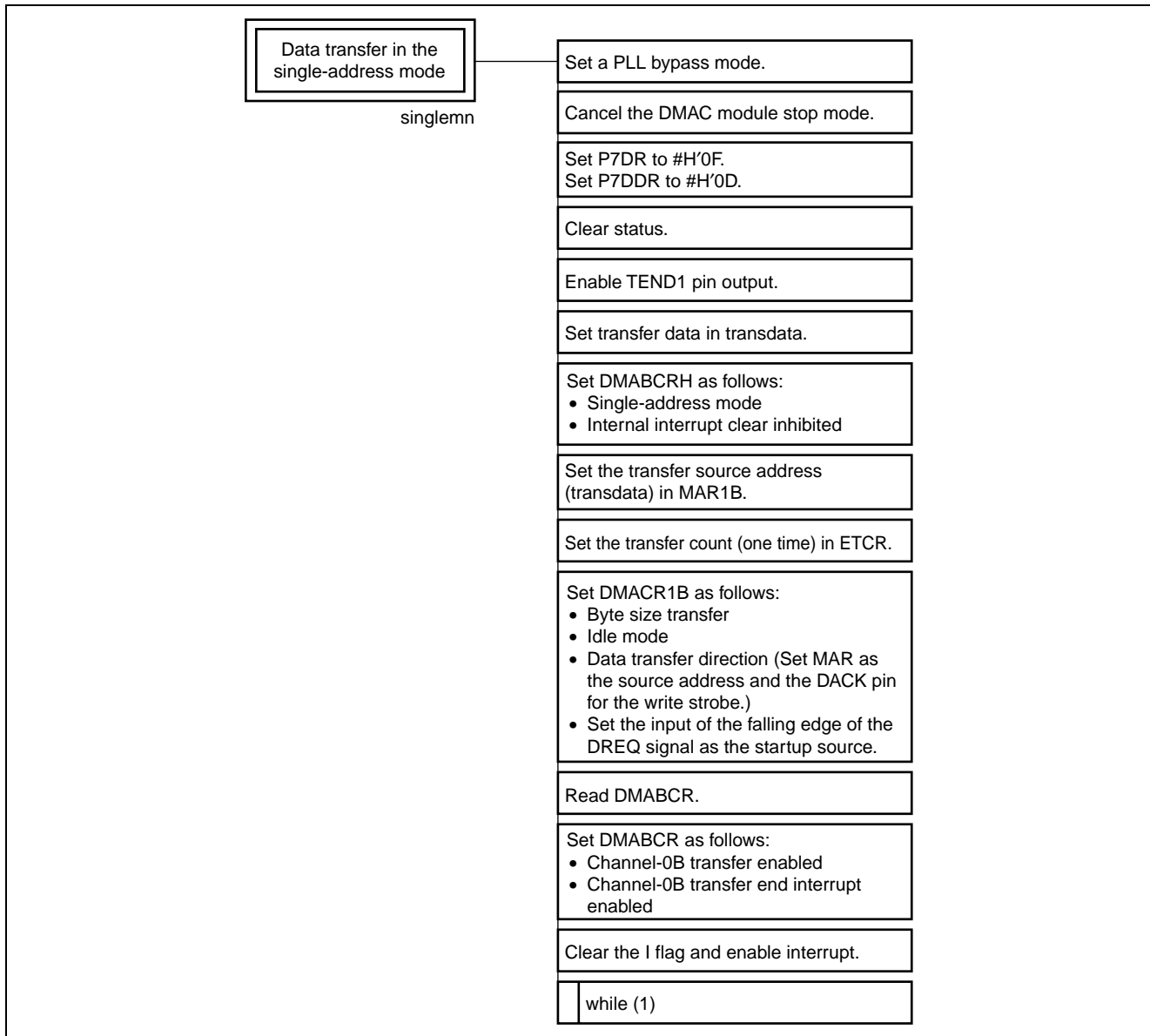
### 4. RAM Usage

Table below describes RAM usage in this sample task.

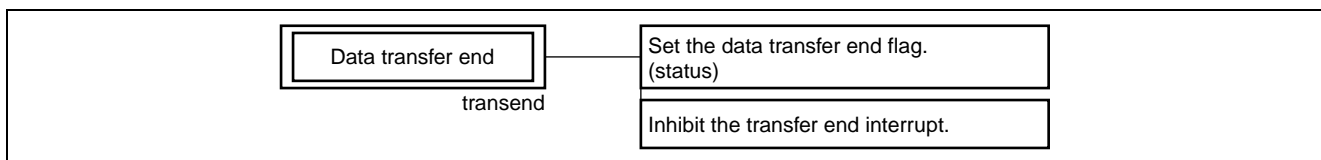
Elements	Function	Data Length	Used in
transdata	Sets data to be transmitted.	unsigned char	Main routine

### 5. PAD

#### 1. Main Routine



#### 2. Data Transfer End



### Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16.04	—	First edition issued

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