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# H8S Family

## Block Transfer

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### Introduction

Outputs data set in ROM to I/O ports and outputs pulse each time a falling edge of an external signal is detected.

### Target Device

H8S/2339

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### 1. Specifications

As shown in figure 1, this sample task transfers 30-byte (6 bytes  $\times$  5 blocks) data set in ROM to I/O ports and outputs pulse each time a falling edge of the external signal IRQ1 is detected.

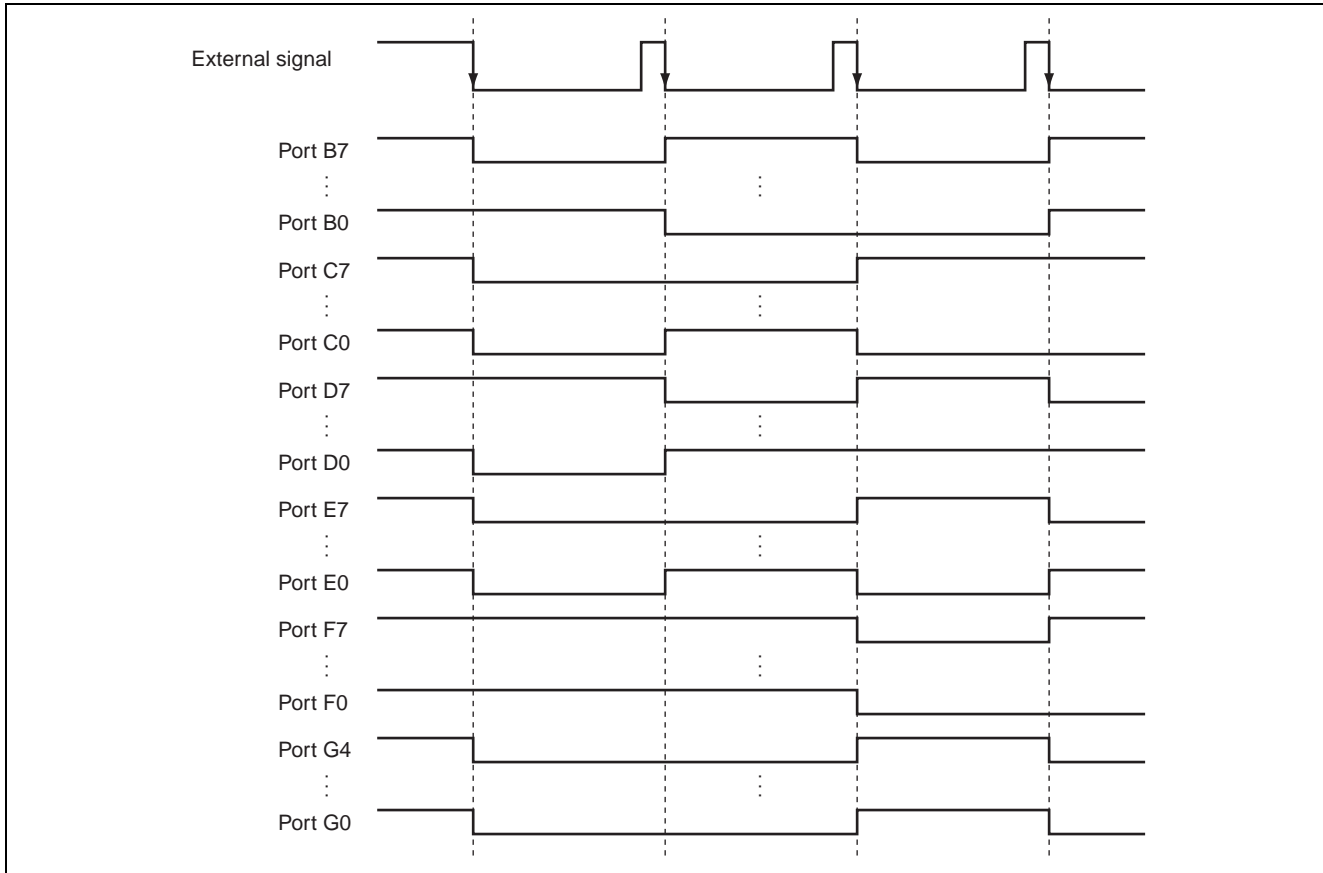


Figure 1 Waveform Output Example

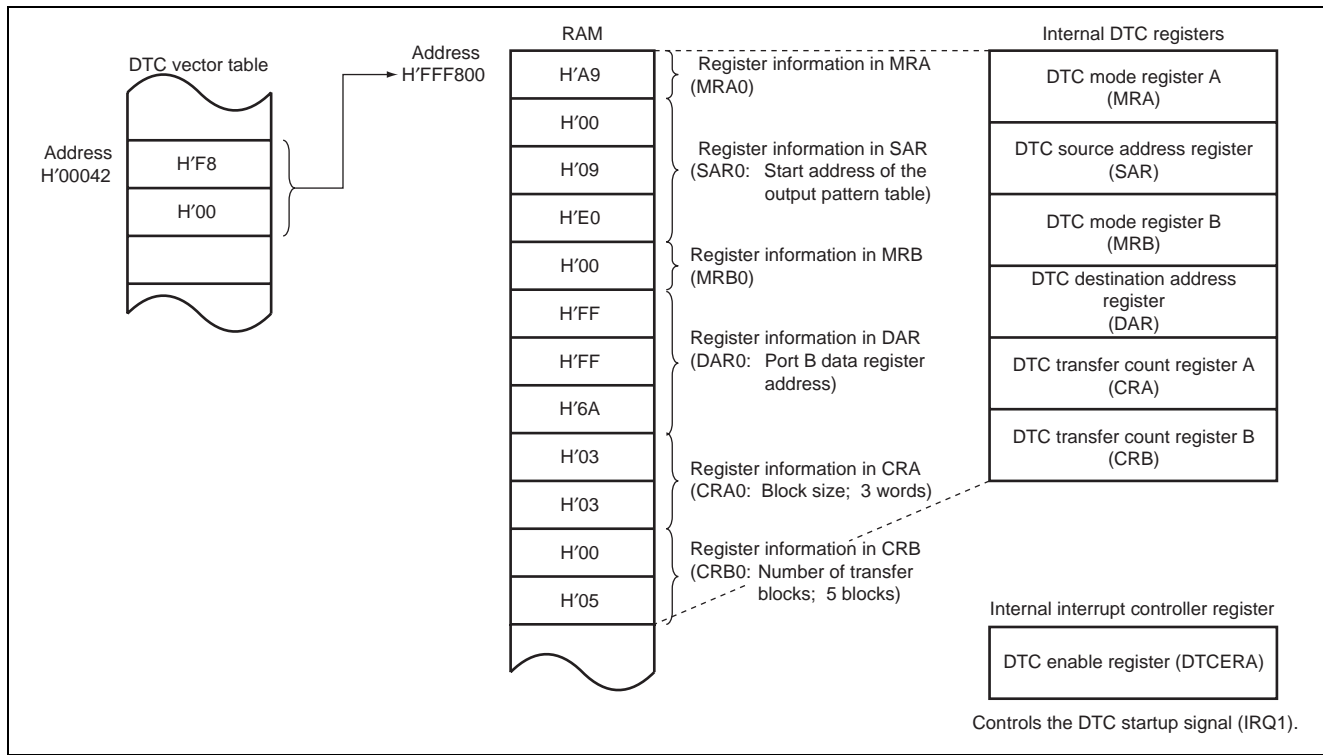
## 2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description
Operating frequency	Input clock: 19.6608 MHz Internal clock: 19.6608 MHz Bus master clock: 19.6608 MHz
MCU clock operating mode	Mode 7 (MD2, MD1, MD0 = 1, 1, 1)



B. The DTC vector table and its allocation in memory are shown in figure 3. DTC register information is allocated in the order of MRA, SAR, MRB, DAR, CRA, and CRB from address H'FFF800.



**Figure 3 DTC Vector Table and Allocation Example in Memory**

### 4. Principles of Operation

1. The principles of operations used of block transfer by DTC are shown in figure 4. This sample task performs hardware and software processing using the timing shown in figure 4 to transfer blocks.

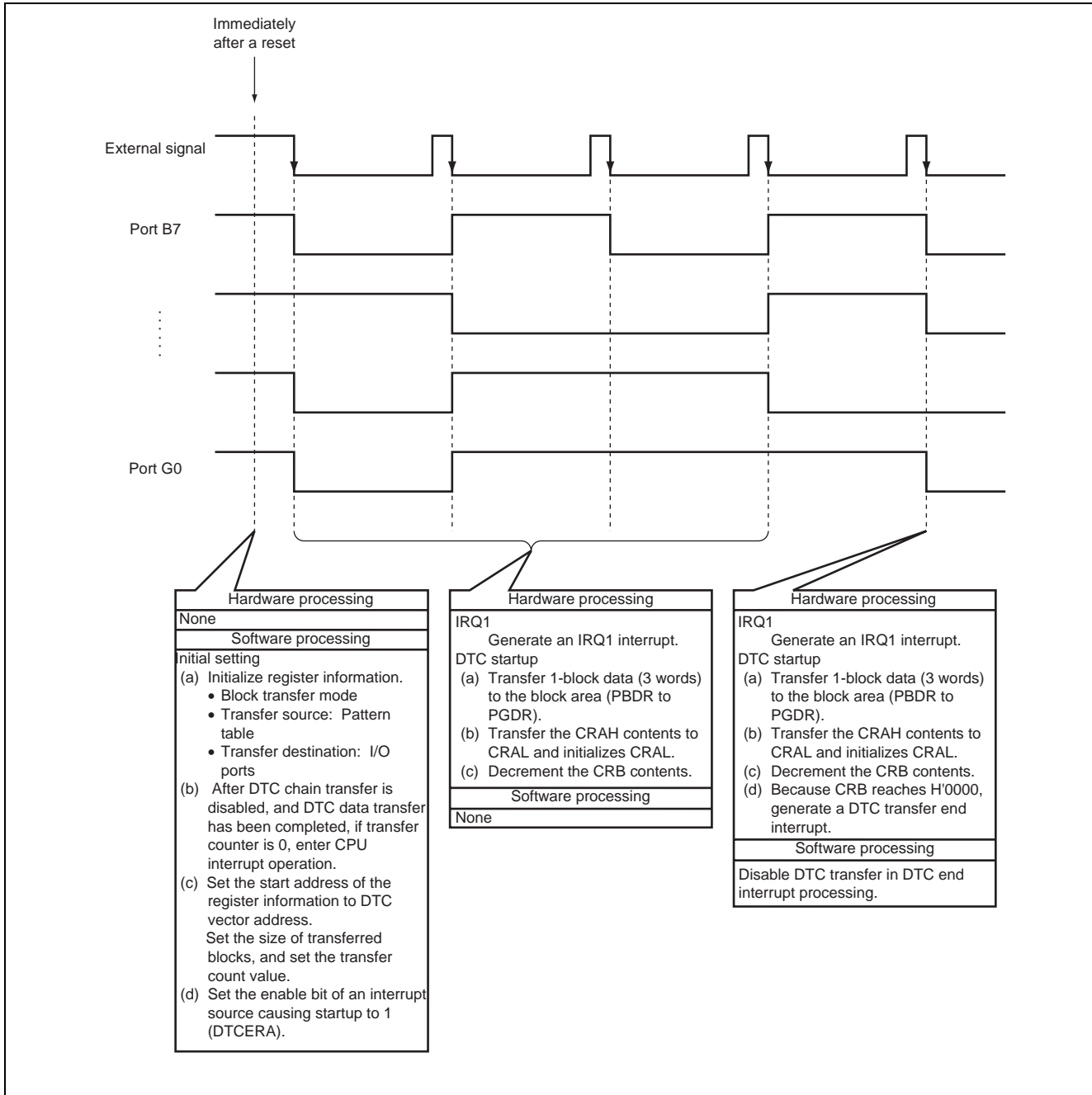


Figure 4 Principles of Operations Used for Block Transfer

## 5. Description of Software

### 1. Description of Modules

Module Name	Label Name	Function
Main routine	blkmn	Performs initial setting for DTC.
Transfer completion routine	txend	Starts up by a DTC transfer end interrupt and disables transfer by DTC.

### 2. Description of Arguments

This sample task uses no inter-module arguments.

### 3. Description of Internal Registers Used

Register Name	Function	Used in
DTCER	Enables DTC startup by an IRQ1 interrupt.	Main routine
MSTPCR	Controls DTC module stop mode.	
ISCR1	Sets an interrupt request at detection of a falling edge of IRQ1.	
IER	Enables an IRQ1 interrupt.	
ISR	Indicates the IRQ1 input status.	

### 4. RAM Usage

Table below describes RAM usage in this sample task.

Label Name	Function	Data Length	Used in
MRA0	Sets DTC0 in block transfer mode, and sets SAR and DAR to be incremented after transfer completion.	unsigned char	Main routine
MRB0	After DTC data transfer completion, if the transfer counter is not 0, disables an interrupt to the CPU.	unsigned char	
SAR0	Sets the transfer source address (PATTBL1).	unsigned long	
DAR0	Sets the transfer destination address (PBDR).	unsigned long	
CRA0	Sets the block size.	unsigned short	
CRB0	Sets the number of blocks to be transferred.	unsigned short	
txendf	Transfer end flag When txend = 0, DTC transfer state, etc. When txend = 1, DTC transfer end.	int	Transfer completion routine

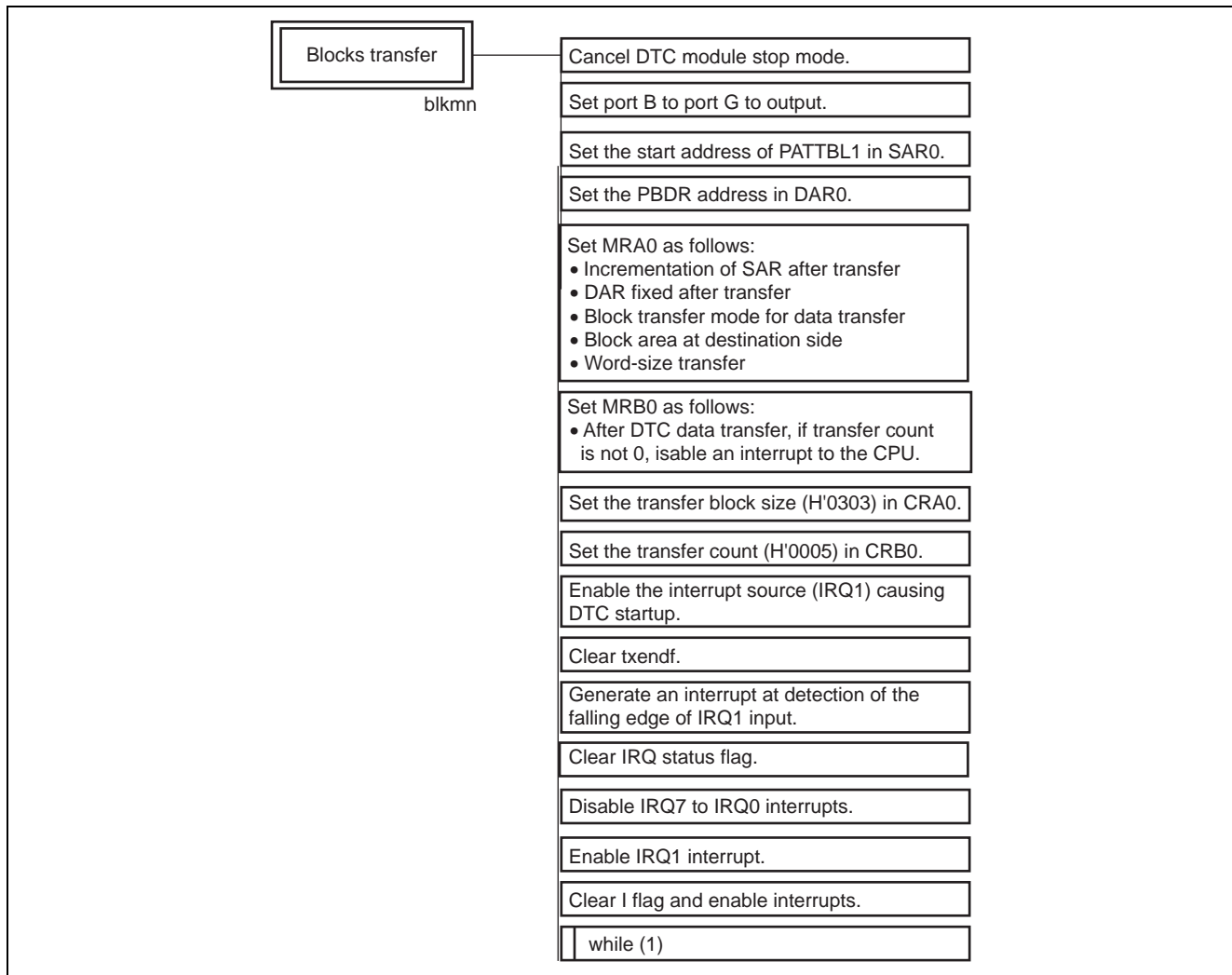
### 5. Description of Data Table

Table Name	Function	Data Length	Data Capacity
PATTBL1	Sets an output pattern.	unsigned short	15 words

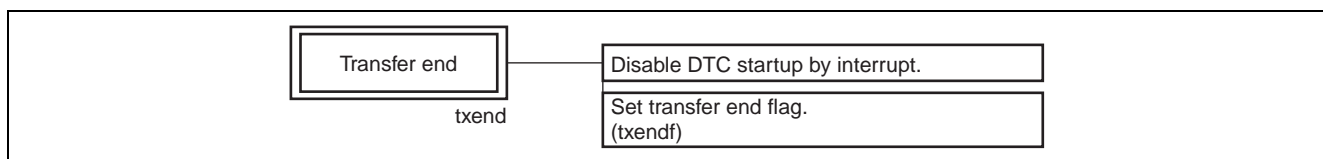
### 6. PAD

#### 6.1 Main Routine and Transfer Completion Routine

##### 1. Main Routine



##### 2. Transfer End



## 6.2 Link Address Specifications

<b>Section Name</b>	<b>Address</b>
CDtc_vect_IRQ1	H'00000422
PResetPRG, PIntPRG, P, C, C\$DSEC, C\$BSEC	H'00000800
B, R	H'00FFDC00
S	H'00FFF9F0

## 6.3 DTC Address Specifications

<b>File Name</b>	<b>DTC Address Specifications</b>
intprg.c	#pragma section Dtc_vect_IRQ1 const unsigned vector_irq1={0xF800};

**Revision Record**

Rev.	Date	Description	
		Page	Summary
1.00	Feb.17.05	—	First edition issued

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