

# H8S Family

## LCD Display Using 1/4 Duty Drive (LCD Controller/Driver)

### Introduction

The segment-type LCD is turned on and off by 1/4 duty drive using the LCD controller/driver and the power-supply circuit.

### Target Device

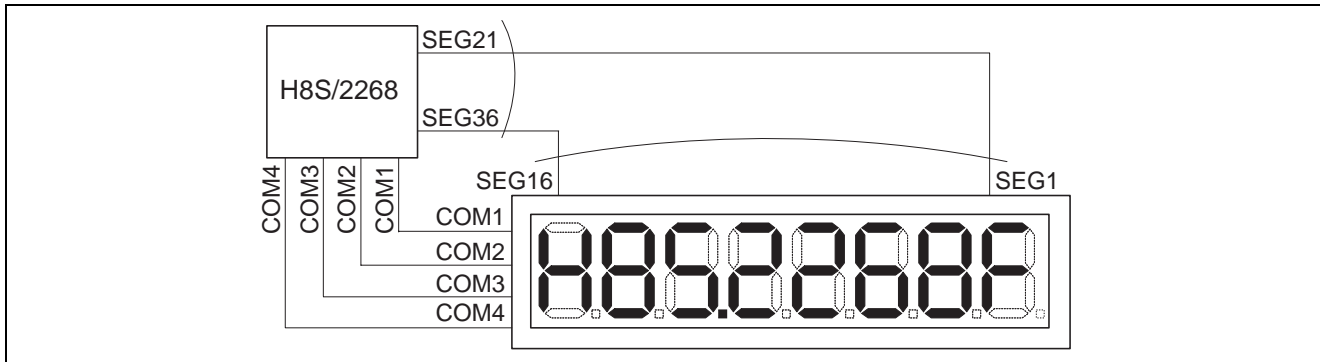
H8S/2268

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## 1. Specifications

- (1) This sample task shows how to use the LCD controller circuit and LCD driver circuit of the H8S/2268 to display information on an LCD module.
- (2) Four common signals and 16 segment signals are used for 1/4 duty display.
- (3) A sample LCD module connection diagram and LCD display example are shown in figure 1.



**Figure 1 Example of LCD Module Connections**

## 2. Functions Used

### (1) Features of LCD Controller/Driver

In this sample task information is displayed on an LCD module using the H8S/2268 internal LCD controller/driver. The features of the LCD controller/driver are listed below.

- Display Capacity
  - (a) Duty cycle: static (internal driver: 40 SEG)
  - (b) Duty cycle: 1/2 (internal driver: 40 SEG)
  - (c) Duty cycle: 1/3 (internal driver: 40 SEG)
  - (d) Duty cycle: 1/4 (internal driver: 40 SEG)
- LCD RAM capacity: 8 bits × 20 bytes (160 bits)
- Byte or word access to LCD RAM is supported.
- The segment output pins can be used as ports in groups of eight.
- In the static mode and with 1/2 duty, common output pins not used because of the duty cycle can be used for common double-buffering (parallel connection).
- A choice of 11 frame frequencies is supported.
- A or B waveform is selectable by software.
- Built-in power supply split-resistors and LCD drive power supply.
- Display is possible in operating modes other than the standby mode and the module stop mode.
- Display is possible during low-voltage operation using built-in triple step-up voltage circuit.
- Module stop mode halts LCD operation when not in use.

(2) Block Diagram of LCD Controller/Driver

A block diagram of the LCD controller/driver used in this sample task is shown in figure 2.

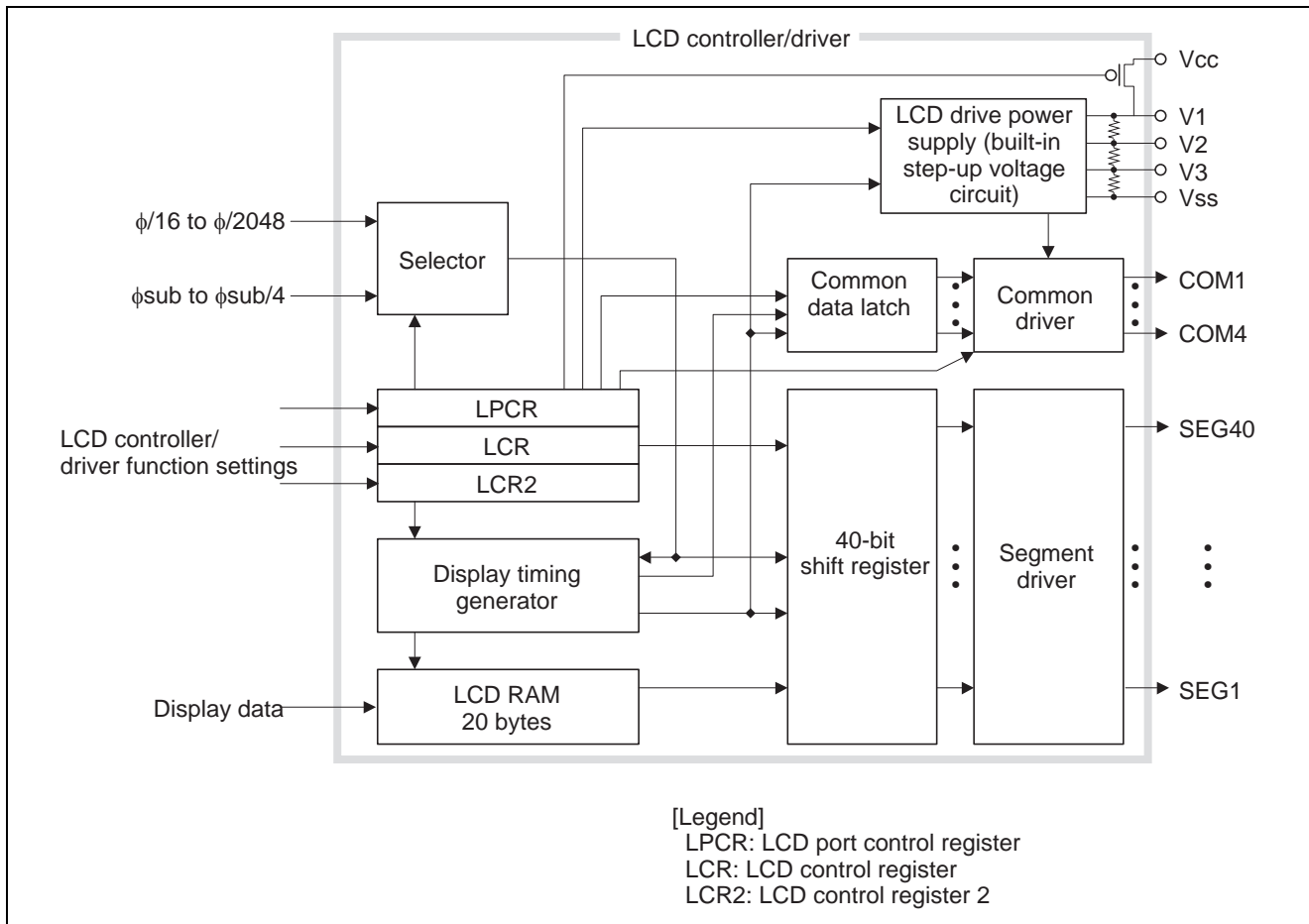


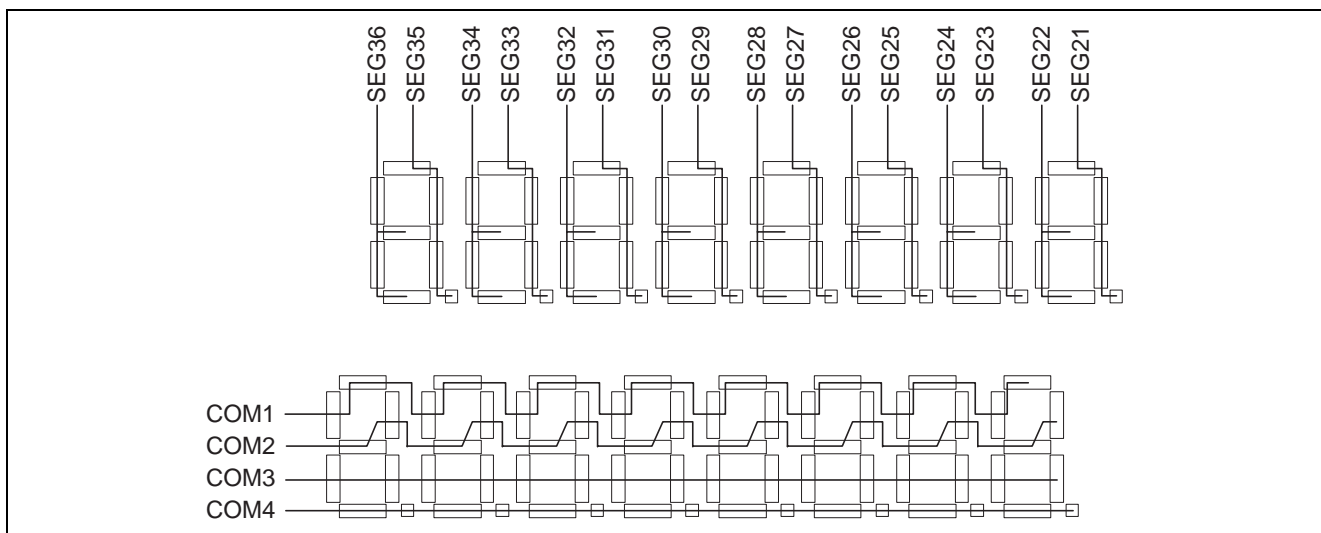
Figure 2 Block Diagram of LCD Controller/Driver

(3) Functions of LCD Controller/Driver

- LCD port control register (LPCR)  
LPCR is an 8-bit readable/writable register that selects the duty cycle, LCD driver, and pin functions.
- LCD control register (LCR)  
LCR is an 8-bit readable/writable register that performs LCD drive power supply on/off control, display function activation control, display data control, and frame frequency selection.
- LCD control register 2 (LCR2)  
LCR2 is an 8-bit readable/writable register that controls switching between the A waveform and B waveform, selects the clock source for the triple step-up voltage circuit, selects the drive power supply, and selects the duty cycle for periods when the power supply split-resistors are connected to the power supply circuit.
- Segment output pins (SEG40 to SEG1)  
These pins are used to drive the LCD segments. All can also function as ports and their settings are programmable.
- Common output pins (COM4 to COM1)  
These are the common drive pins for the LCD. In the static mode and with 1/2 duty, these pins can be used in parallel.
- LCD power supply pins (V1, V2, V3)  
These pins are used when the H8S/2268 is connected to a bypass capacitor, and an external power supply is used. The V3 pin functions as the reference power supply input to the LCD when the triple step-up voltage circuit is used.
- LCD step-up voltage capacitance pins (C1, C2)  
These are the capacitance pins for the LCD drive power supply step-up voltage.
- LCD RAM  
Used to set the display data. The relationship between LCD RAM and the display segments differs depending on the duty cycle. After setting the registers required for display, data is written to the portions of LCD RAM corresponding to the duty cycle using normal RAM instructions. Display begins automatically when the LCD is powered on. Word- or byte-access instructions may be used for RAM setting.

(4) Connection Diagram

In this sample task an 8-digit 8-segment LCD and 1/4 duty cycle are used for LCD display. A connection diagram for the segment signals and common signals for the 8-digit 8-segment LCD used in the sample task is shown in figure 3.



**Figure 3 Connection Diagram for Segment Signals and Common Signals for 8-Digit 8-Segment LCD Used in Sample Task**

### (5) LCD RAM Map

A map of LCD RAM for 1/4 duty cycle operation is shown in figure 4.

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
H'FFFC40	SEG2	SEG2	SEG2	SEG2	SEG1	SEG1	SEG1	SEG1
H'FFFC41	SEG4	SEG4	SEG4	SEG4	SEG3	SEG3	SEG3	SEG3
H'FFFC42	SEG6	SEG6	SEG6	SEG6	SEG5	SEG5	SEG5	SEG5
H'FFFC43	SEG8	SEG8	SEG8	SEG8	SEG7	SEG7	SEG7	SEG7
H'FFFC44	SEG10	SEG10	SEG10	SEG10	SEG9	SEG9	SEG9	SEG9
H'FFFC45	SEG12	SEG12	SEG12	SEG12	SEG11	SEG11	SEG11	SEG11
H'FFFC46	SEG14	SEG14	SEG14	SEG14	SEG13	SEG13	SEG13	SEG13
H'FFFC47	SEG16	SEG16	SEG16	SEG16	SEG15	SEG15	SEG15	SEG15
H'FFFC48	SEG18	SEG18	SEG18	SEG18	SEG17	SEG17	SEG17	SEG17
H'FFFC49	SEG20	SEG20	SEG20	SEG20	SEG19	SEG19	SEG19	SEG19
H'FFFC4A	SEG22	SEG22	SEG22	SEG22	SEG21	SEG21	SEG21	SEG21
H'FFFC4B	SEG24	SEG24	SEG24	SEG24	SEG23	SEG23	SEG23	SEG23
H'FFFC4C	SEG26	SEG26	SEG26	SEG26	SEG25	SEG25	SEG25	SEG25
H'FFFC4D	SEG28	SEG28	SEG28	SEG28	SEG27	SEG27	SEG27	SEG27
H'FFFC4E	SEG30	SEG30	SEG30	SEG30	SEG29	SEG29	SEG29	SEG29
H'FFFC4F	SEG32	SEG32	SEG32	SEG32	SEG31	SEG31	SEG31	SEG31
H'FFFC50	SEG34	SEG34	SEG34	SEG34	SEG33	SEG33	SEG33	SEG33
H'FFFC51	SEG36	SEG36	SEG36	SEG36	SEG35	SEG35	SEG35	SEG35
H'FFFC52	SEG38	SEG38	SEG38	SEG38	SEG37	SEG37	SEG37	SEG37
H'FFFC53	SEG40	SEG40	SEG40	SEG40	SEG39	SEG39	SEG39	SEG39
	↓	↓	↓	↓	↓	↓	↓	↓
	COM4	COM3	COM2	COM1	COM4	COM3	COM2	COM1

**Figure 4 Map of LCD RAM for 1/4 Duty Cycle**

### (6) Relationship between LCD Display and LCD RAM Setting Values

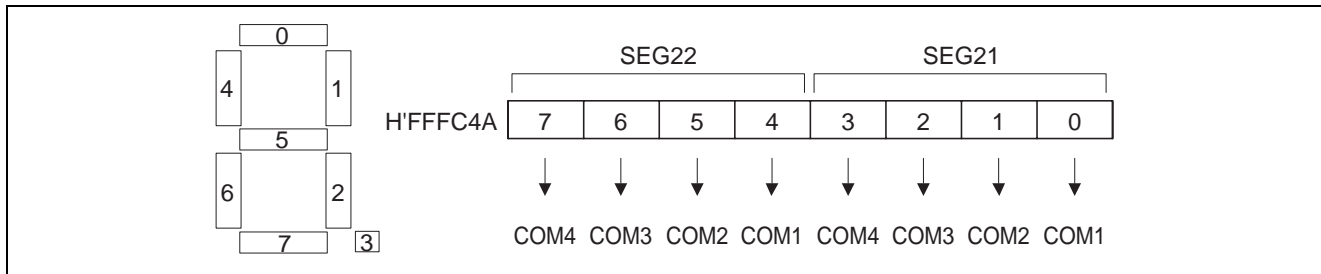
The relationship between the information displayed on the 8-digit 8-segment LCD used in this sample task and the LCD RAM setting values is shown in figure 5. Figure 5 shows the values set in the LCD RAM used to display "H8S.2268F" on the 8-digit 8-segment LCD.

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
H'FFFC51	0	1	1	1	0	1	1	0	Display data for "H "
H'FFFC50	1	1	1	1	0	1	1	1	Display data for "8 "
H'FFFC4F	1	0	1	1	1	1	0	1	Display data for "S."
H'FFFC4E	1	1	1	0	0	0	1	1	Display data for "2 "
H'FFFC4D	1	1	1	0	0	0	1	1	Display data for "2 "
H'FFFC4C	1	1	1	1	0	1	0	1	Display data for "6 "
H'FFFC4B	1	1	1	1	0	1	1	1	Display data for "8 "
H'FFFC4A	0	1	1	1	0	0	0	1	Display data for "F "

**Figure 5 Relationship between LCD Display and LCD RAM Setting Values**

### (7) LCD Display/Non-Display

The relationship between SEG21 and SEG22 of the 8-digit 8-segment LCD and the corresponding values set in the LCD RAM is shown in figure 6. As shown in figure 6, a setting of 1 for a bit in LCD RAM for a segment from 0 to 7 causes the corresponding segment to display, and a setting of 0 causes non-display.



**Figure 6 Relationship between LCD Display/Non-Display and Corresponding LCD RAM Setting Values**

**(8) Display Data Examples**

Display examples for SEG21 and SEG22 of the 8-digit 8-segment LCD and the corresponding display data are shown in table 1.

**Table 1 Display Data Examples**

Symbol	Display	Address	Display Data							
			Binary number							Hexadecimal number
		H'FFFC4A	0	0	0	0	0	0	0	H'00
-		H'FFFC4A	0	0	1	0	0	0	0	H'20
.		H'FFFC4A	0	0	0	0	1	0	0	H'08
0		H'FFFC4A	1	1	0	1	0	1	1	H'D7
1		H'FFFC4A	0	0	0	0	0	1	1	H'06
2		H'FFFC4A	1	1	1	0	0	0	1	H'E3
3		H'FFFC4A	1	0	1	0	0	1	1	H'A7
4		H'FFFC4A	0	0	1	1	0	1	1	H'36
5		H'FFFC4A	1	0	1	1	0	1	0	H'B5
6		H'FFFC4A	1	1	1	1	0	1	0	H'F5
7		H'FFFC4A	0	0	0	0	0	1	1	H'07
8		H'FFFC4A	1	1	1	1	0	1	1	H'F7
9		H'FFFC4A	1	0	1	1	0	1	1	H'B7
A		H'FFFC4A	0	1	1	1	0	1	1	H'77
B		H'FFFC4A	1	1	1	1	0	1	0	H'F4
C		H'FFFC4A	1	1	0	1	0	0	0	H'D1
D		H'FFFC4A	1	1	1	0	0	1	1	H'E6
E		H'FFFC4A	1	1	1	1	0	0	0	H'F1
F		H'FFFC4A	0	1	1	1	0	0	0	H'71

(9) Assignment of Functions

Assignment of functions in this sample task is shown in table 2.

**Table 2 Assignment of Functions**

Elements	Description
LPCR	Selects the duty cycle, the LCD driver, and pin functions.
LCR	Performs LCD power supply on/off control, display function activation control, display data control, and frame frequency selection.
LCR2	Controls switching between the A and B waveforms, selects the clock source for triple step-up voltage circuit, selects drive power supply, and selects duty cycle for periods when power supply split-resistors are connected to the power supply circuit.
SEG36 to SEG21	Used to drive the LCD segments
COM4 to COM1	Used as common drivers
LCD RAM	Sets LCD display data (addresses H'FFFC40 to H'FFFC53)

### 3. Principles of Operation

#### (1) Hardware Settings

##### (a) LCD Drive Power Supply Settings

The H8S/2268 supports use of its built-in power supply circuit, or use of an external power supply circuit, as the LCD drive power supply. If an external power supply circuit is used as the LCD drive power supply, connect the V1 pin to the external power supply.

##### (b) Triple Step-up Voltage Circuit

The H8S/2268 uses a triple step-up voltage circuit so that a voltage three times the LCD input reference voltage from the V3 pin can be used to drive the LCD. In this sample task operation of the triple step-up voltage circuit is turned off (the SUPS bit = 0).

#### (2) Software Settings

The software settings for implementing LCD display are described below.

##### (a) Selecting the Duty Cycle and Common Function

The DTS1 and DTS0 bits are used to select the duty cycle setting from among static mode, 1/2 duty, 1/3 duty, and 1/4 duty. The CMX bit is used to select the common double-buffering function.

##### (b) Selecting the Segment Drivers

The SGS3 to SGS0 bits are used to select the segment drivers to be used.

##### (c) Selecting the Frame Frequency

The CKS3 to CKS0 bits are used to select the frame frequency. Select a frame frequency that matches the specifications of the LCD module used.

##### (d) Selecting A Waveform or B Waveform

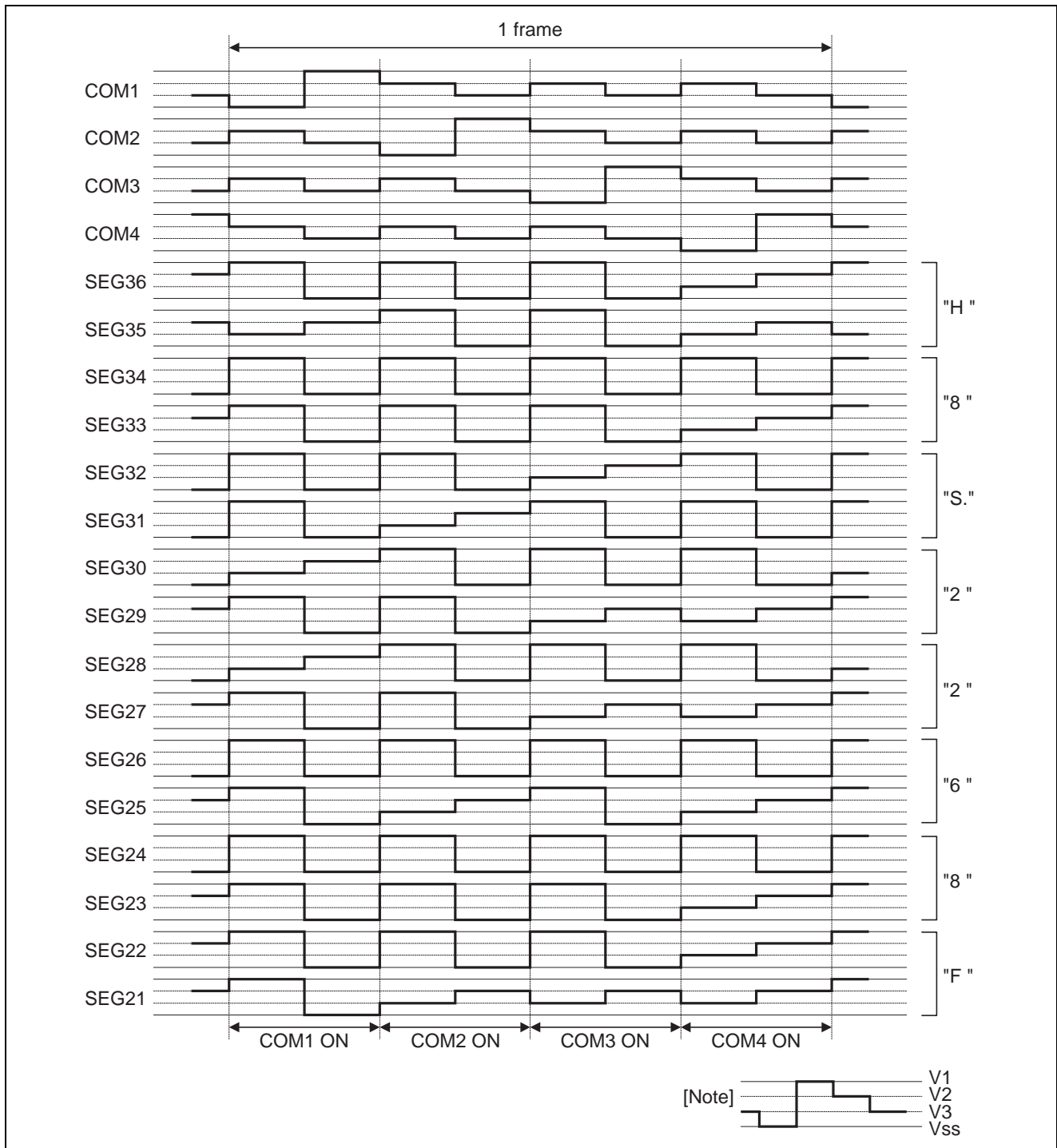
The LCDAB bit is used to select the A waveform or the B waveform as the LCD waveform.

##### (e) Selecting the LCD Drive Power Supply

The SUPS bit can be used to select the power supply if the internal power supply circuit is used. To use an external power supply circuit, select  $V_{CC}$  using SUPS and turn the LCD drive power supply off using the PSW bit.

### (3) Principles of Operation

The principles of operation of this sample task are illustrated in figure 7.



**Figure 7 Principles of Operation**

## 4. Description of Software

### (1) Modules

Table 3 shows the modules used in this sample task.

**Table 3 Modules**

Module	Label	Description
Main routine	main	Performs initial settings for LCD RAM and LCD controller/driver, and displays information on LCD

### (2) Arguments

No arguments are used in this sample task.

### (3) Internal Registers Used

The internal registers used in this sample task are shown in table 4.

**Table 4 Internal Registers Used**

Register	Bit Name	Description	Address	Set Value
LPCR		LCD port control register	H'FFFC30	H'C3
	DTS1	Duty cycle select 1 and 0	Bit 7	DTS1 = 1
	DTS0	The combination of DTS1 and DTS0 selects static mode, or 1/2, 1/3, or 1/4 duty. <ul style="list-style-type: none"> <li>DTS1 = 1, DTS0 = 1: 1/4 duty selected</li> </ul>	Bit 6	DTS0 = 1
	CMX	Common function select Specifies whether or not the same waveform is to be output from multiple pins to increase the common drive power when not all common pins are used because of the duty setting. <ul style="list-style-type: none"> <li>CMX = 0: Same waveform not output from multiple common pins not used because of duty setting</li> <li>CMX = 1: Same waveform output from multiple common pins not used because of duty setting</li> </ul>	Bit 5	0
	SGS3	Segment driver select 3 to 0	Bit 3	SGS3 = 0
SGS2	These bits select the segment drivers to be used.	Bit 2	SGS2 = 0	
SGS1	<ul style="list-style-type: none"> <li>SGS3 = 0, SGS2 = 0, SGS1 = 1, SGS0 = 1: Pins</li> </ul>	Bit 1	SGS1 = 1	
SGS0	SEG40 to SEG17 function as segment drivers and SEG16 to SEG1 function as port pins	Bit 0	SGS0 = 1	

**Table 4 Internal Registers Used (cont)**

Register	Bit Name	Description	Address	Set Value
LCR		LCD control register	H'FFFC1	H'31
	PSW	LCD power supply split-resistor connection control This bit can be used to disconnect the LCD power supply split-resistors from $V_{CC}$ when LCD display is not required in a power-down mode or when an external power supply is used. When the ACT bit is cleared to 0, and also in the standby mode, the LCD power supply split-resistors are disconnected from $V_{CC}$ regardless of the setting of this bit. <ul style="list-style-type: none"> <li>PSW = 0: LCD power supply split-resistors are disconnected from <math>V_{CC}</math></li> <li>PSW = 1: LCD power supply split-resistors are connected to <math>V_{CC}</math></li> </ul>	Bit 6	0
	ACT	Display function activate This bit specifies whether or not the LCD controller/driver is used. Clearing this bit to 0 halts operation of the LCD controller/driver. The LCD drive power supply is also turned off, regardless of the setting of the PSW bit. However, register contents are retained. <ul style="list-style-type: none"> <li>ACT = 0: LCD controller/driver operation disabled</li> <li>ACT = 1: LCD controller/driver operation enabled</li> </ul>	Bit 5	1
	DISP	Display data control This bit specifies whether the contents of LCD RAM are displayed or blank data is displayed regardless of the LCD RAM contents. <ul style="list-style-type: none"> <li>DISP = 0: Blank data is displayed</li> <li>DISP = 1: LCD RAM data is displayed</li> </ul>	Bit 4	1
CKS3	Frame frequency select 3 to 0	Bit 3	CKS3 = 0	
CKS2	These bits select the clock source and frame frequency.	Bit 2	CKS2 = 0	
CKS1		Bit 1	CKS1 = 1	
CKS0	<ul style="list-style-type: none"> <li>CKS3 = 0, CKS2 = 0, CKS1 = 0, CKS0 = 1: <math>\phi_{SUB}/2</math> selected as the clock source and 64 Hz selected as the frame frequency</li> </ul>	Bit 0	CKS0 = 1	

**Table 4 Internal Registers Used (cont)**

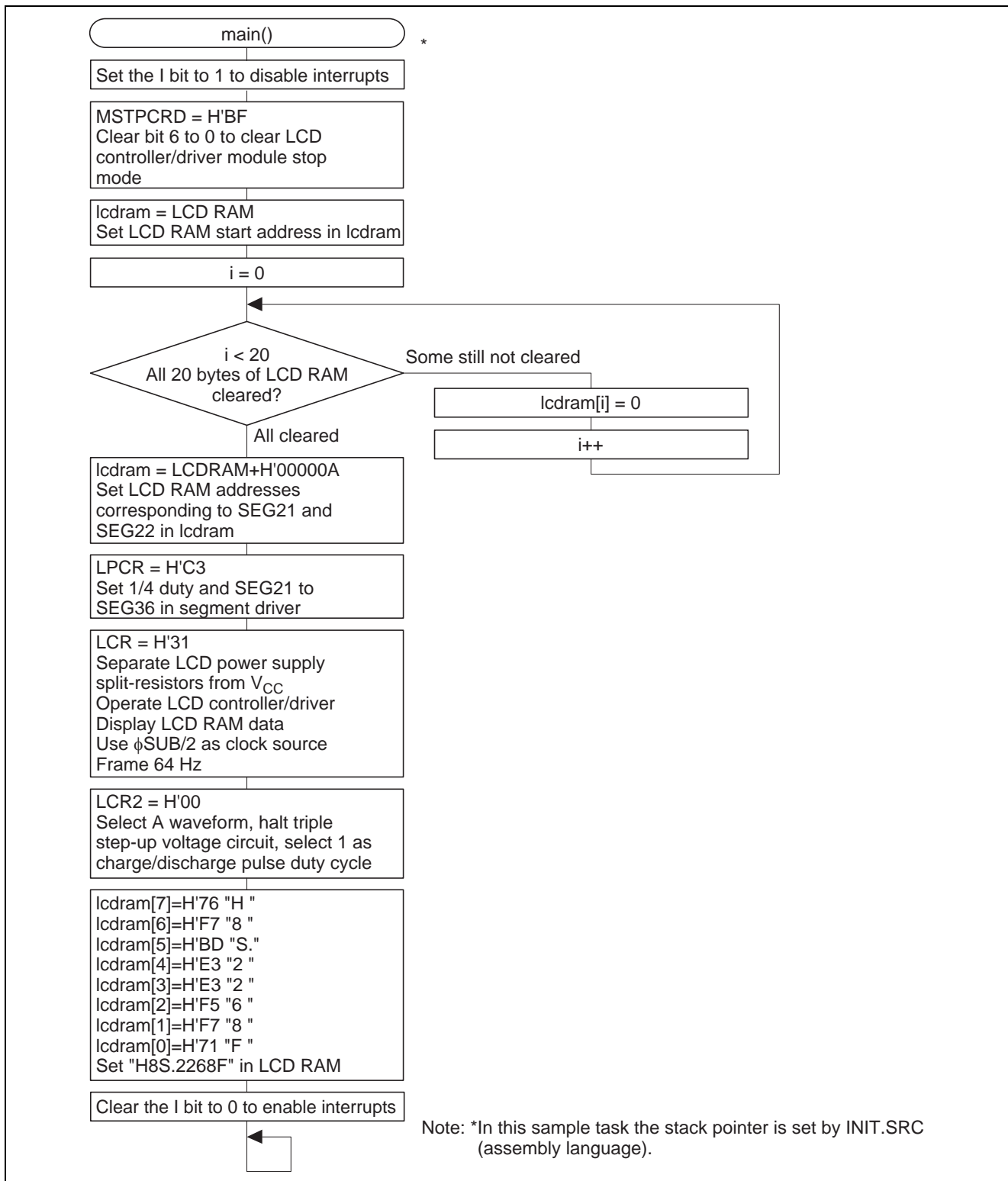
Register	Bit Name	Description	Address	Set Value
LCR2		LCD control register 2	H'FFFC2	H'00
	LCDAB	A waveform/B waveform switching control Specifies whether the A waveform or B waveform is used as the LCD drive waveform. <ul style="list-style-type: none"> <li>LCDAB = 0: Drive using the A waveform</li> <li>LCDAB = 1: Drive using the B waveform</li> </ul>	Bit 7	0
	HCKS	Triple step-up voltage circuit clock select Selects the clock used for the triple step-up voltage circuit. This bit selects a clock which is equivalent to the clock specified by the LCD operating control register (LCR) divided by 4 or 8 as the step-up voltage circuit clock. <ul style="list-style-type: none"> <li>HCKS = 0: Clock equivalent to LCD operating clock divided by 4 selected as step-up voltage circuit clock</li> <li>HCKS = 1: Clock equivalent to LCD operating clock divided by 8 selected as step-up voltage circuit clock</li> </ul>	Bit 5	0
	SUPS	Drive power select, triple step-up voltage circuit control The triple step-up voltage circuit stops operating when V <sub>CC</sub> is selected as the drive power supply. The triple step-up voltage circuit starts operating when the LCD input reference voltage (VLCD3) is selected as the drive power supply. <ul style="list-style-type: none"> <li>SUPS = 0: Drive power supply is V<sub>CC</sub>, triple step-up voltage circuit halts</li> <li>SUPS = 1: Drive power supply is triple step-up voltage of the LCD input reference voltage (VLCD3); triple step-up voltage circuit operates</li> </ul>	Bit 4	0
	CDS3	Selection of duty cycle for charge/discharge pulse	Bit 3	CDS3 = 0
	CDS2	Selects the duty cycle for periods when the power supply divider resistance is connected to the power supply circuit. A duty cycle of 0 specifies a fixed state in which the power supply divider resistance is separated from the power supply circuit. Therefore, it is necessary to supply power to pins V1, V2, and V3 from an external circuit. <ul style="list-style-type: none"> <li>CDS3 = 0, CDS2 = 0, CDS1 = 0, CDS0 = 0: Duty cycle = 1</li> </ul>	Bit 2	CDS2 = 0
	CDS1		Bit 1	CDS1 = 1
	CDS0		Bit 0	CDS0 = 1
MSTPCRD		Module stop control register D	H'FFF60	H'BF
	MSTPD6	<ul style="list-style-type: none"> <li>MSTPD6 = 0: LCD controller/driver module stop mode cleared</li> <li>MSTPD6 = 1: LCD controller/driver module stop mode set</li> </ul>	Bit 6	0

(4) RAM Usage

No RAM is used in this sample task.

## 5. Flowchart

### (1) Main Routine



## 6. Program Listings

INIT. SRC program listing

```
.export _INIT
.import _main
;
.section P, CODE, ALIGN=2
_INIT:
mov.l #h'ffefc0, er7
ldc.b #b'10000000, ccr
ldc.b #0, exr
jmp @_main
;
.end
```

```

/*****
/*
/* H8S/2000 Series -H8S/2268-
/* Application Note
/*
/* 'Liquid Crystal Display
/* -1/4 Duty Drive, Internal Driver-'
/*
/* Function
/* : LCD Controller / Driver
/*
/* External Clock : 10MHz
/* Internal Clock : 10MHz
/* Sub Clock : 32.768kHz
/*
/*****
#include <machine.h>
/*****
/* Symbol Definition
/*****
#define LPCR *(volatile unsigned char *)0xFFFC30 /* LCD Port Control Register */
#define LCR *(volatile unsigned char *)0xFFFC31 /* LCD Control Register */
#define LCR2 *(volatile unsigned char *)0xFFFC32 /* LCD Control Register 2 */
#define LCD RAM (volatile unsigned char *)0xFFFC40 /* LCD RAM */
#define MSTPCRD *(volatile unsigned char *)0xFFFC60 /* Module Stop Control Registers D */
/*****
/* Function define
/*****
extern void INIT ( void ); /* SP Set */
void main ( void );
/*****
/* Vector Address
/*****
#pragma section V1 /* VECTOR SECTOIN SET */
void (*const VEC_TBL1[])(void) = { /* 0x00 - 0x0f */
INIT /* 00 Reset */
};
#pragma section /* P */

```

```

/*****/
/* Main Program */
/*****/
void main ( void )
{
int i;
unsigned char *LCD RAM;
set_imask_ccr(1); /* Interrupt Disable */
MSTPCRD = 0xBF; /* module stop mode is cleared */
LCD RAM = LCD RAM;
for ( i = 0; i < 20; i++ ){ /* Initialize LCD RAM */
LCD RAM[i] = 0;
}
LCD RAM = LCD RAM + 0x00000A; /* Set LCD RAM Address */
LPCR = 0xC3; /* 1/4 Duty / SEG40-SEG17 ON */
LCR = 0x31; /* LCD ON / Phi_sub/2 */
LCR2 = 0x00; /* A waveform / Drive power is Vcc */
LCD RAM[7] = 0x76; /* "H " */
LCD RAM[6] = 0xF7; /* "8 " */
LCD RAM[5] = 0xBD; /* "S." */
LCD RAM[4] = 0xE3; /* "2 " */
LCD RAM[3] = 0xE3; /* "2 " */
LCD RAM[2] = 0xF5; /* "6 " */
LCD RAM[1] = 0xF7; /* "8 " */
LCD RAM[0] = 0x71; /* "F " */
set_imask_ccr(0); /* Interrupt Enable */
while(1);
}

```

## 7. Link Addresses

Section	Address
CV1	H' 000000
P	H' 000100

### Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.09.05	—	First edition issued

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