

# MAEC TECHNICAL NEWS No.M16C-71-0105

## Setting procedure of processor mode bits

### Classification

Corrections and supplementary explanation of document

- ✓ Notes
- Knowhow
- Others

### Products Effected

M16C/80 Series  
M16C/60 Series

## 1. Precautions

Processor mode bits are allocated to bits 1 and 0 of the processor mode register 0. Regardless of the level of the CNVss pin, changing the processor mode bits selects the mode. Therefore, never change the processor mode bits when changing the contents of other bits. Do not change the processor mode bits simultaneously with other bits when changing the processor mode bits "012" or "112". Change the processor mode bits after changing the other bits.

Figure 1 shows the processor mode register 0 of M16C/62A group, and figure 2 shows the setting procedure of processor mode bits.

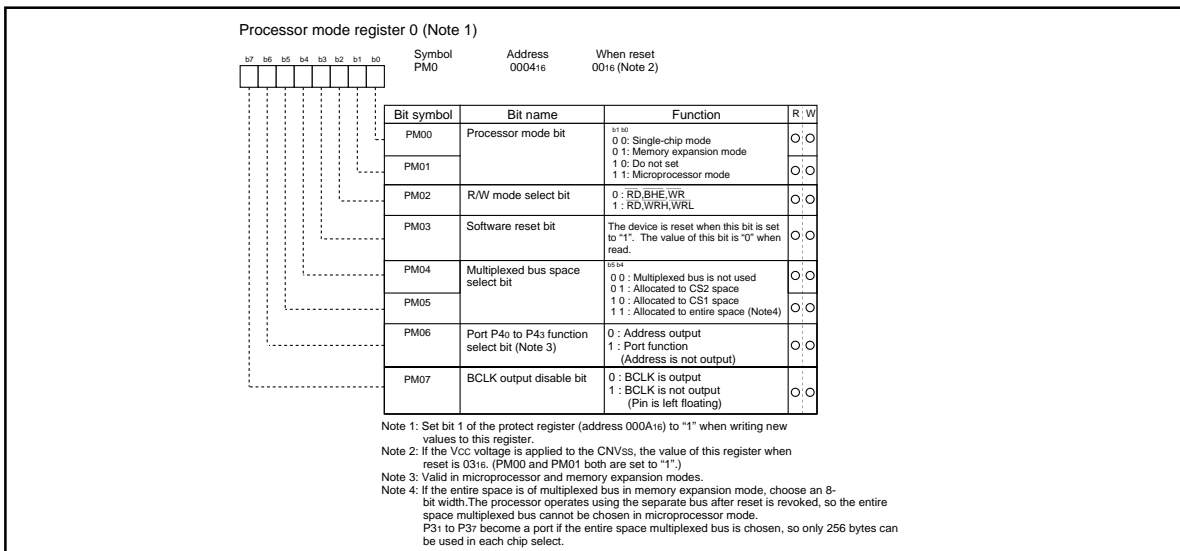


Figure 1. Processor mode register 0

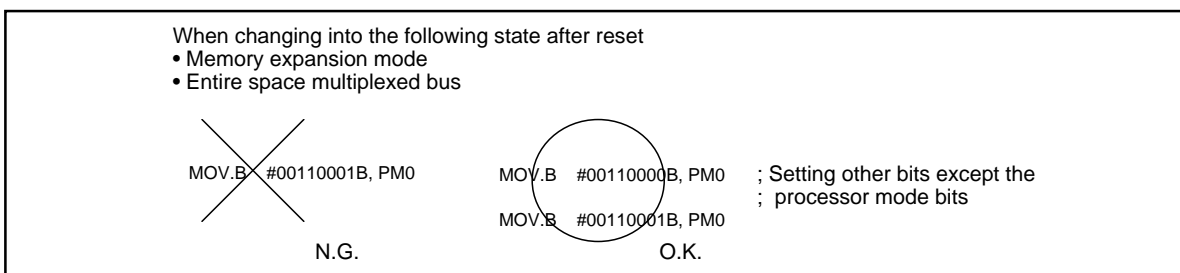


Figure 2. Setting procedure