



R0P7145TH001MRK

General Information Manual

RENESAS SH7145 μ T-Engine specification board set

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[Precaution for Safety]

In both the General Information Manual and on the product itself, several icons are used to insure proper handling of this product and also to prevent injuries to you or other persons, or damage to your properties.

This chapter describes the precautions which should be taken in order to use this product safely and properly. Be sure to read this chapter before using this product.

	This symbol represents a warning about safety. It is used to arouse caution about a potential danger that will possibly inflict an injury on persons. To avoid a possible injury or death, please be sure to observe the safety message that follows this symbol.
 DANGER	DANGER indicates an imminently dangerous situation that will cause death or heavy wound unless it is avoided. However, there are no instances of such danger for the product presented in this user's manual.
 WARNING	WARNING indicates a potentially dangerous situation that will cause death or heavy wound unless it is avoided.
 CAUTION	CAUTION indicates a potentially dangerous situation that will cause a slight injury or a medium-degree injury unless it is avoided.
CAUTION	CAUTION with no safety warning symbols attached indicates a potentially dangerous situation that will cause property damage unless it is avoided.
IMPORTANT	This is used in operation procedures or explanatory descriptions to convey exceptional conditions or cautions to the user.

In addition to the five above, the following are also used as appropriate.

△means WARNING or CAUTION. Example:  CAUTION AGAINST AN ELECTRIC SHOCK
⊘means PROHIBITION. Example:  DISASSEMBLY PROHIBITED
●means A FORCIBLE ACTION. Example:  UNPLUG THE POWER CABLE FROM THE RECEPTACLE.

⚠WARNING

Warning for AC Power Supply:



If the attached AC Power cable does not fit the receptacle, do not alter the AC power cable and do not plug it forcibly. Failure to comply may cause electric shock and/or fire.

Use an AC power cable which complies with the safety standard of the country.

Do not touch the plug the AC power cable when your hands are wet. This may cause electric shock.

This product is connected signal ground with frame ground. If your developing product is transformless (not having isolation transformer of AC power), this may cause electric shock. Also, this may give an unrepairable damage to this product and your developing one.

While developing, connect AC power of the product to commercial power through isolation transformer in order to avoid these dangers.

If other equipment is connected to the same branch circuit, care should be taken not to overload the circuit.



When installing this equipment, insure that a reliable ground connection is maintained.



If you smell a strange odor, hear an unusual sound, or see smoke coming from this product, then disconnect power immediately by unplugging the AC power cable from the outlet.

Do not use this as it is because of the danger of electric shock and/or fire, In this case, contact your local distributor.

Before setting up this product and connecting it to other devices, turn off power a remove a power cable to prevent injury or product damage.

Warning to Be Taken for This Product:



Do not disassemble or modify this product. Personal injury due to electric shock may occur if this product is disassembled and modified. Disassembling and modifying the product will void your warranty.

Make sure nothing falls into the cooling fan on the top panel, especially liquids, metal objects, or anything combustible.

Warning for Installation:



Do not set this product in water or areas of high humidity. Make sure that product does not get wet. Spilling water or some other liquid into the product may cause unrepairable damage.

Warning for Use Environment:



This equipment is to be used in an environment with a maximum ambient temperature of 35°C. Care should be taken that this temperature is not exceeded.

⚠ CAUTION**Note on Connecting the Power Supply:**

Do not use any power cable other than the one that is included with the product.

The power cable included with the product has its positive and negative poles color-coded by red and black, respectively.

Pay attention to the polarities of the power supply. If its positive and negative poles are connected in reverse, the internal circuit may be broken.

Do not apply any voltages exceeding the product's rated power supply voltage ($5.0V \pm 5\%$). Extreme voltages may cause a burn due to abnormal heat or cause the internal circuit to break down.

Cautions to Be Taken for Handling This Product:

Use caution when handling the main unit. Be careful not to apply a mechanical shock.

Do not touch the connector pins of the product main unit and the target MCU connector pins directly.

Excessive flexing or force of the flexible cable for connecting this product to the emulation probe may break connector.

Cautions to Be Taken for System Malfunctions:

If the product malfunctions because of interference like external noise, do the following to remedy the trouble.

(1) Press the RESET button on the board.

(2) If normal operation is not restored after step (1), shut OFF the product once and then reactivate it.

[MEMO]

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Chapter 1. Product Overview

1.1 Content of the Package

This product consists of the boards and components listed in the table below. After unpacking your product, please check to see that all items are included.

Table1.1 List of Package Contents

Type name	Description	Quantity
μT-Engine board	CPU board and debug board	1 pc. each
AC adapter	Power supply	1
Serial cable	Dedicated serial cable	1
CD-ROM	<ul style="list-style-type: none"> · SH7145 μT-Engine board user's manual · μT-Engine/SH7145 development kit software and related documents 	1
Guide to user registration	Written in Japanese	1
μT-Engine/SH7145 development kit software usage conditions	Written in Japanese	1

* Please keep the packing box and cushioning materials of the product. You can use them when you send your product for repair or for other purposes. In that case, make sure the product is handled as precision equipment during transport. If other means of transport are used for an unavoidable reason, make sure the product is packed firmly as precision equipment.

* If there is any question or doubt about the content of the package, please contact your nearest office of Renesas Technology Corporation, Renesas Solutions Corporation, or Renesas Technology Sales Co., Ltd. or its distributor.

* Use an AC adapter which complies with the safety standard of the country.

1.2 System Configuration

1.2.1 System Configuration

Figure 1.1 shows a system configuration in which the product is used. Items other than the μ T-Engine board and its attachments are expected to be prepared by users.

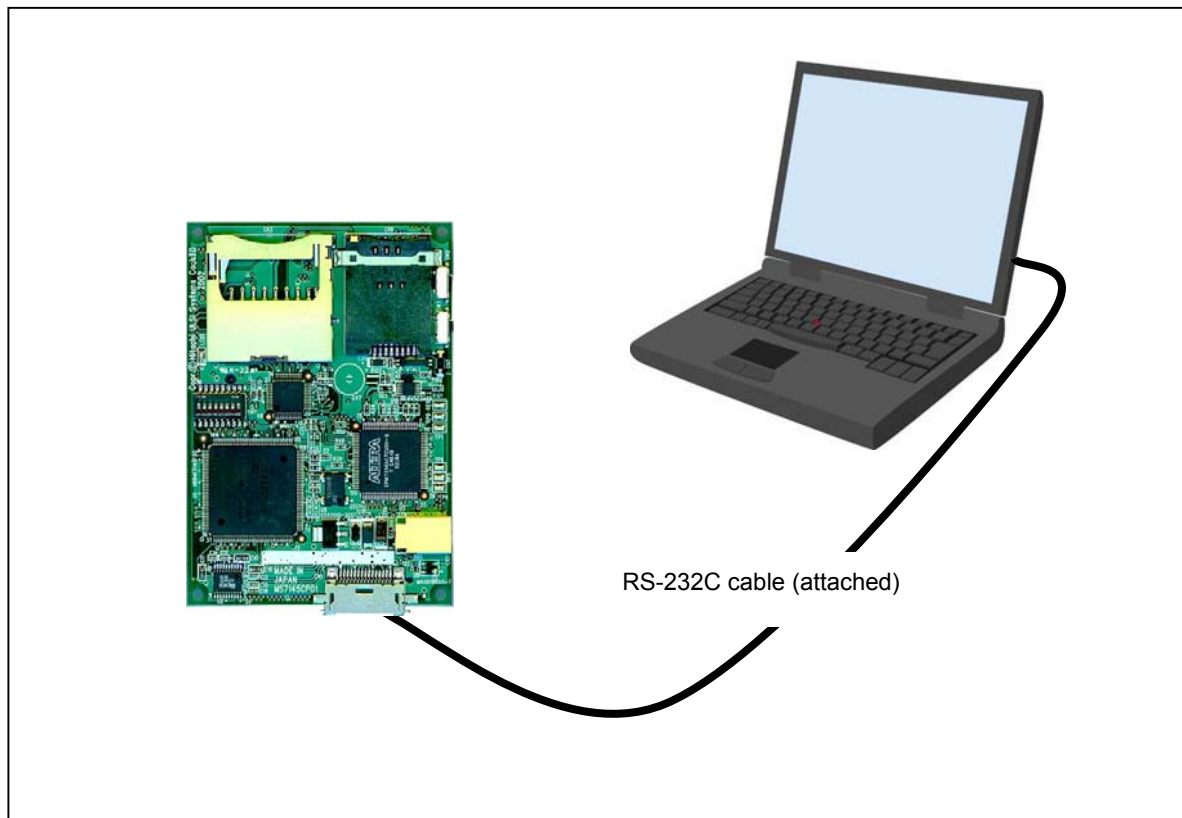


Figure 1.1 System Configuration

1.2.2 Name and Function of Each Part of the μ T-Engine Board

Figure 1.2 shows an external view of the μ T-Engine board. Figures 1.3-(A) and (B) show the name of each part of the board.

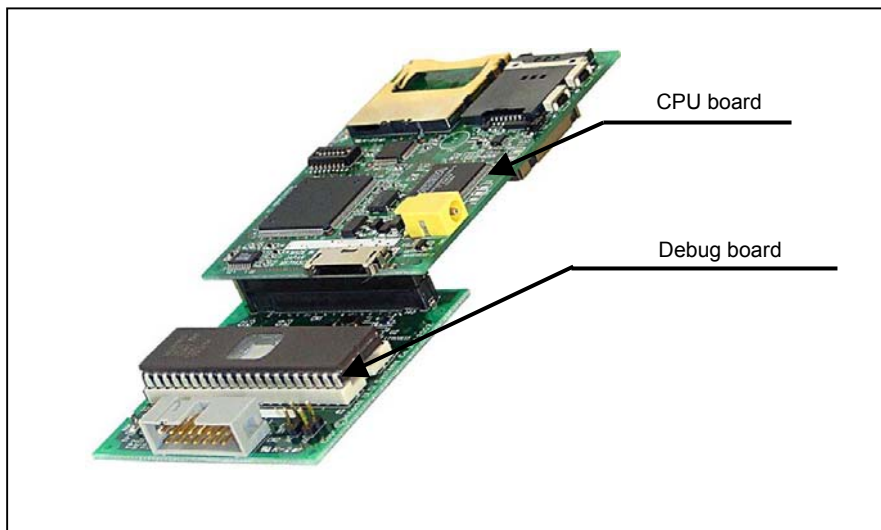


Figure 1.2 External View of the μ T-Engine Board

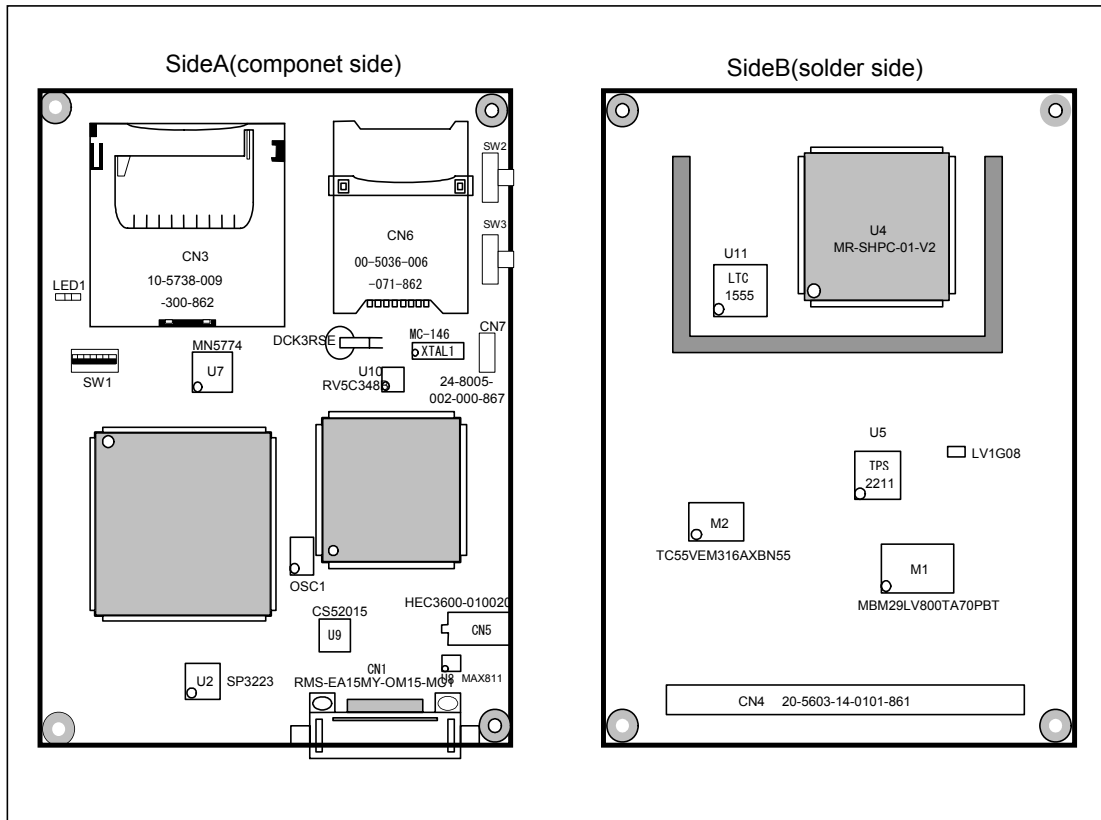


Figure 1.3-(A) CPU Board

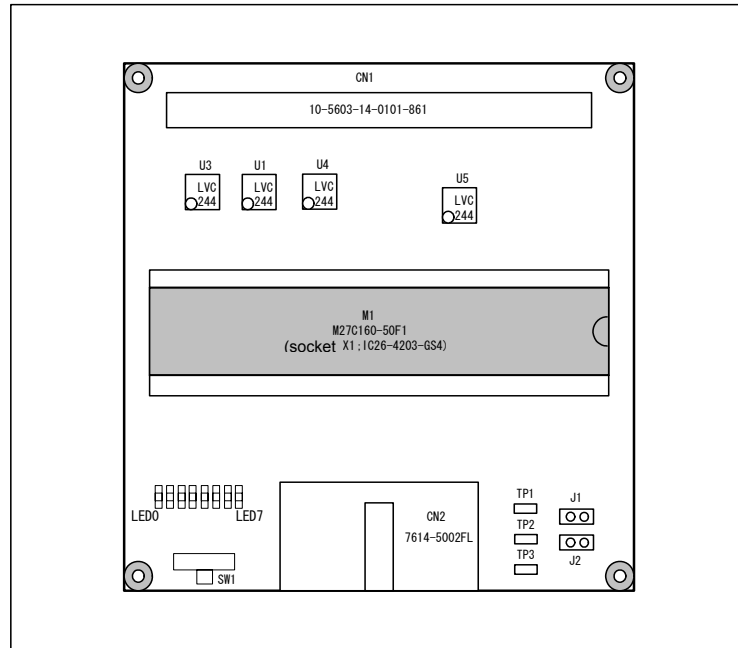


Figure 1.3-(B) Debug board

1.3 Specifications

Table 1.1 lists the functional specifications of the μ T-Engine board.

Table 1.1 Functional Specifications of the μ T-Engine Board

Item	Specification	remarks
CPU	SH7145 Type name:HD64F7145F50(Renesas Technology) Input clock:12.5MHz Operating clock:50MHz(frequency multiplied by 2) Package:144pin LQFP	
Flash Memory	Capacity:1MB MBM29LV800TA70PBT(Fujitsu) \times 1	
SRAM	Capacity:1MB TC55VEM316AXBN55 (Toshiba) \times 1	
CF Card I/F	1Slot Controller:MR-SHPC-01 V2T(Marubun) Package:144pin TQFP	
SD Card I/F	1Slot Controller:MN5774(Matsushita) Package:48pin TQFP	
RTC	Type name:RV5C348B(RICOH) Package:10pin SSOP-G	

1.4 Working Environment Conditions

Table 1.2 lists the working environment conditions under which the μ T-Engine board can be used. Table 1.3 lists the permissible amount of current that can be supplied from each power supply of the board to external devices.

Table 1.2 Ambient Environment Conditions

Item	Specification
Environment	Operating conditions <ul style="list-style-type: none"> • Temperature: 10 to 35°C • Humidity: 30 to 85%RH (no dewdrops allowed) • Must be free of ambient gas and corrosive gas
Operating voltage	5.6V DC
Current consumption	400mA
Dimensions	CPU board: 85 mm x 60 mm Debug board: 60 mm x 60 mm

Table 1.3 Permissible Amount of Current that Can be Supplied to the Outside

Power supply voltage	Permissible amount of current	Power can be supplied to
3.3V	500mA	<ul style="list-style-type: none"> • CF card power supply • Expansion slot

CAUTION

Regarding the working environment conditions:



- The “current consumption” in Table 1.2 indicates the maximum amount of current consumed in the μ T-Engine board (CPU board and debug board) when it is operating singly.
- The “permissible amount of current” of each power supply in Table 1.3 refers to the total amount of current supplied to external devices. If a CF card consumes 100 mA of current, for example, then the amount of current usable by expansion slots is 500 mA – 100 mA = 400 mA.
- If the internal power supply of the μ T-Engine board is fed to CF cards, etc., make sure the “permissible amount of current” of each power supply in Table 1.3 is not exceeded. Excessive use of power beyond the maximum amount of current may cause an electrical shock, generation of heat, or a fire.

[MEMO]

Chapter 2. Setting Up

2.1 Connecting the Board and Host System

To use the monitor program, connect the μ T-Engine board and the host system by plugging the attached RS-232C interface cross cable into the serial interface connector (CN1) on the μ T-Engine board. Figure 2.1 shows how to connect the μ T-Engine board and the host system.

Figure 2.2 shows the pin arrangement of the serial interface connector. Table 2.1 lists signal assignments of the serial interface connector.

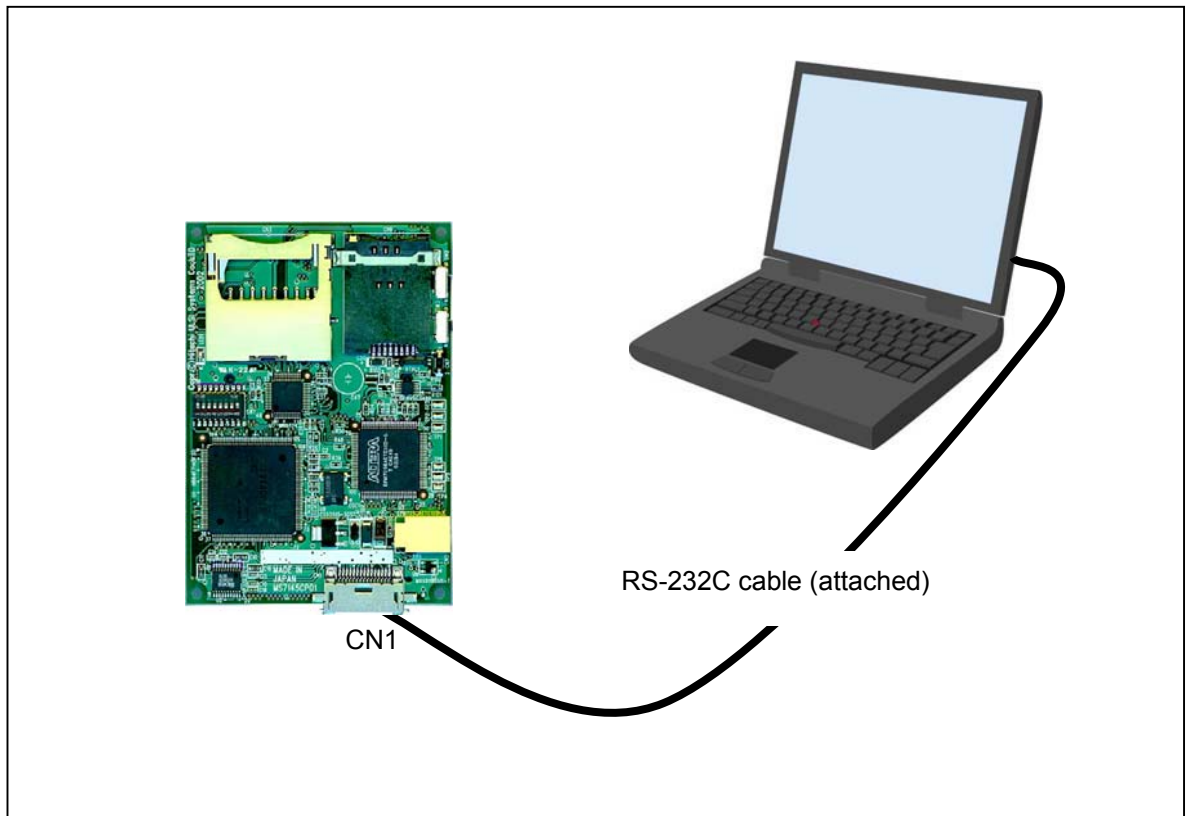


Figure 2.1 Connecting the Board and Host System

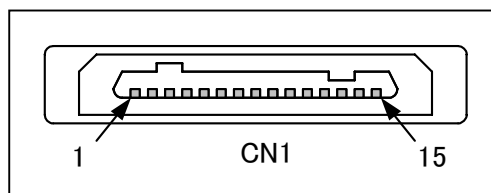


Figure 2.2 Pin Arrangement of the Serial Interface Connector

Table 2.1 Signal Assignments of the Serial Interface Connector

Pin No.	Signal name	Input/Output	Remark
1	GND	—	
2	TxD	Output	TXB(UART)
3	RxD	I	RXB(UART)
4	GND	—	
5	RTS	O	RTSB(UART)
6	CTS	I	CTSB(UART)
7	GND	—	
8	Reserved	—	ISP TCK(*)
9	Reserved	—	GND(*)
10	Reserved	—	ISP TMS(*)
11	Reserved	—	ISP Plug(*)
12	Reserved	—	ISP BScan(*)
13	Reserved	—	ISP TDI(*)
14	Reserved	—	ISP TDO(*)
15	Reserved	—	Vcc(3.3V) (*)

* The signals marked with an asterisk (*) are used to test the board when it is shipped from the factory. Do not connect any devices to these signals.

2.2 Connecting the AC Adapter

(1) About the Power Supply

The power supply that can be used with this product must be the following specifications.

- Plug : EIAJ RC-5320A Voltage Classification 2
- Input Voltage : DC 5.6V
- Polarity : Outside : negative (-) polarity. Center : positive (+).

(2) Connecting

Figure 2.3 shows how to connect the AC adapter to the μ T-Engine board. To connect the AC adapter, insert the adapter plug into the AC adapter connector on the μ T-Engine (1), and then insert the other end of the AC adapter into an AC outlet (2), as shown in Figure 2.3.

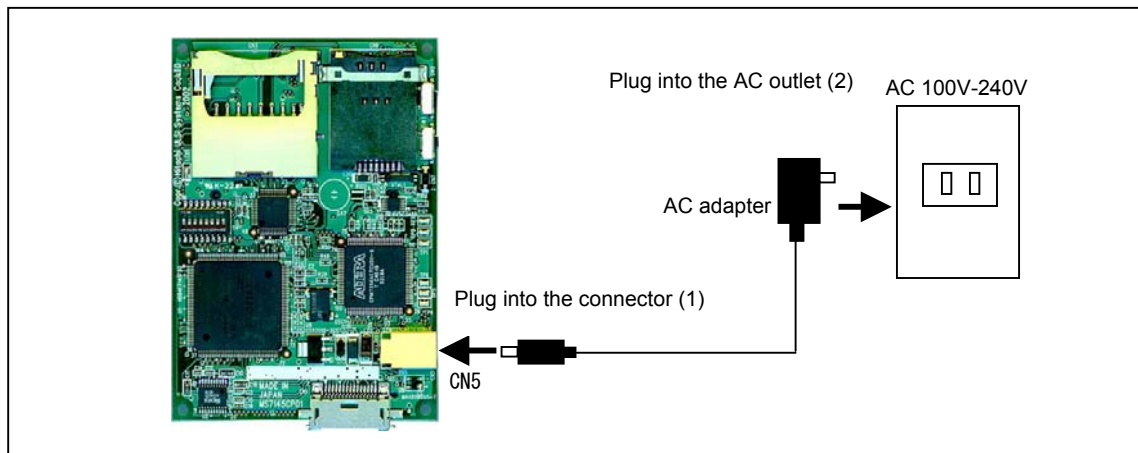


Figure 2.3 Connecting the AC Adapter

⚠ CAUTION

Regarding power supply connections:



Do not place heavy articles on the AC adapter cord, or damage, break, or modify it. Such an act may cause a fire or electric shock due to a leakage of electricity.

Do not hold the plug of the AC adapter with wet hands when you connect or disconnect it, because you may get an electric shock. When you disconnect the AC adapter, be sure to pull the plug, not the cord. If you pull the cord, it may be damaged and cause electric shock or fire.

Before plugging the AC adapter into the wall outlet, check the cables, etc. that they are connected correctly again. If Wrong connections may cause an electric shock, fire or malfunction.

Use an AC adapter which complies with the safety standard of the country.

2.3 Powering On/Off the μ T-Engine Board

To turn the power to the μ T-Engine board on or off, press the power-on switch (SW2) on the CPU board.

Holding down this switch for 0.5 seconds or more turns the power to the board on. Conversely, when you hold down this switch for 2 seconds or more while the power to the μ T-Engine board is on, the board is powered off.

2.4 Using the Debug Board

2.4.1 Functions of the Debug Board

When the debug board is connected to the μ T-Engine board, you can make use of its functions described below.

- (1) The internal flash memory of the μ T-Engine board can be rewritten by running the program that is written into the EPROM in the debug board. For details on how to rewrite, refer to Chapter 9, "Rewriting the Flash Memory."
- (2) The 8-bit LEDs on the debug board can be turned on or off under control from ports on the SH7145. The running status of software can be monitored by controlling the LEDs to turn on and off.
- (3) An H-UDI debugger that uses the H-UDI pin of the SH7145 can be connected.

2.4.2 Connecting the Debug Board

Figure 2.4 shows how to connect the debug board to the μ T-Engine board. Use the expansion slot (CN4) on the μ T-Engine board to connect the debug board.

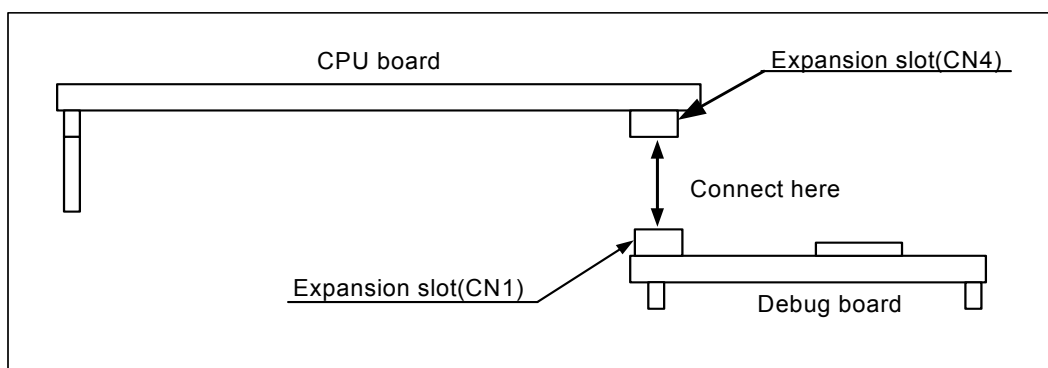


Figure 2.4 Connecting the Debug Board to the μ T-Engine Board

⚠ CAUTION

Regarding the debug board and EPROM connection:



Turn off the power to the μ T-Engine board before connecting EPROM to the debug board. When you reconnect EPROM, check to see that the direction in which you are going to connect it is correct, as shown in Figure 2.5.

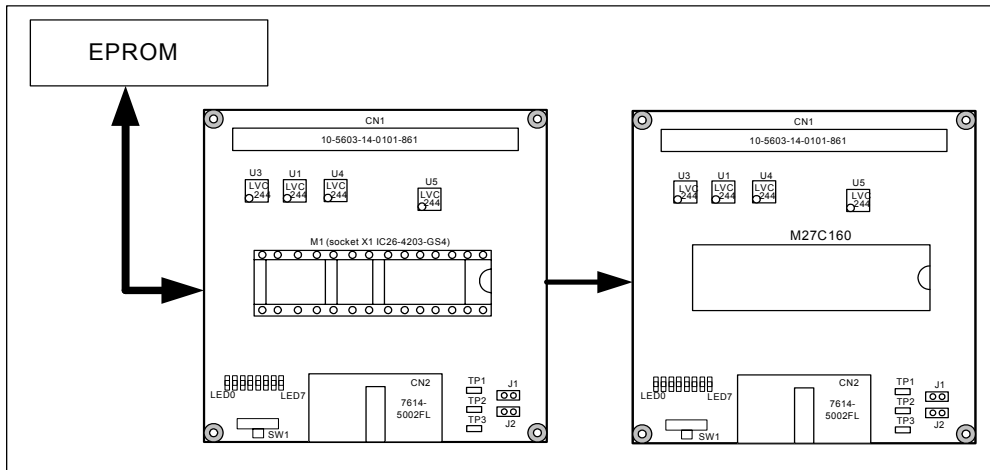


Figure 2.5 Connecting EPROM

2.4.3 Jumper Switches on the Debug Board

Table 2.2 shows how the EPROM select jumper switch (J1) on the debug board should be set. Note, however, that this setting is for the case where the SH7145 operates in mode 0.

Table 2.3 shows how the jumper switch used for H-UDI debugger connection (J2) should be set.

For details about a memory map of the SH7145 when the debug board is connected in the system, refer to Chapter 4, “Memory Map.”

Table 2.2 Jumper Switch Settings for EPROM Selection

Jumper switch	Setting	Description
J1	<p>1-2 open</p>	<p>The resources of the debug board should be located in area 0 of the SH7145, as shown below. (Factory default)</p> <ul style="list-style-type: none"> - Allocate the flash memory of the CPU board to the addresses h'00000000 to h'000FFFFF. - Allocate the EPROM of the debug board to the addresses h'00100000 to h'002FFFFF.
	<p>1-2 shorted</p>	<p>The resource of the debug board should be located in area 0 of the SH7145, as shown below.</p> <ul style="list-style-type: none"> - Allocate the EPROM of the debug board to the addresses h'00000000 to h'001FFFFF. - Allocate the flash memory of the CPU board to the addresses h'00200000 to h'002FFFFF.

Table 2.3 Jumper Switch Settings for H-UDI Debugger Connection

Jumper switch	Setting	Description
J2	<p>1-2 open</p>	<p>Set the ASEMD pin of the SH7145 to the high level. (Factory default) The SH7145 operates in normal mode.</p>
	<p>1-2 shorted</p>	<p>Set the ASEMD pin of the SH7145 to the low level. An H-UDI debugger can be used.</p>

CAUTION

Regarding jumper settings:



Always be sure to turn off the power to the μ T-Engine board before you alter jumper settings on it or connect a cable to the board. This is necessary to prevent the internal circuit of the board from breaking down.

2.4.4 8-bit LEDs on the Debug Board

The 8-bit LEDs on the debug board connect to the SH7145's port D consisting of 8 bits (PD16–19 and PD28–31). The LEDs can be turned on or off by writing data to the port D. The LED for the bit to which data "1" is written goes out, and the LED for the bit to which data "0" is written lights up.

2.4.5 NMI Switch on the Debug Board

SW1 on the debug board is a pushbutton switch to control NMIs of the SH7145. Pressing this switch causes the NMI pin to go low, and releasing the switch causes the NMI pin to go high.

2.4.6 Connecting a H-UDI Debugger

The debug board allows an H-UDI debugger to be connected to its 14-pin H-UDI connector (CN2). This H-UDI connector connects to the H-UDI pin of the SH7145. Figure 2.6 shows how to connect an H-UDI debugger. Plug the cable extending from the H-UDI debugger into the H-UDI connector (CN2) on the debug board.

Note that only a specific type of H-UDI debugger can be connected to the μ T-Engine board, as designated below. For details on how to connect an H-UDI debugger and how to set it up, refer to the instruction manual included with the debugger.s

- E10A-USB emulator, type name: HS0005KCU01H (H-UDI only)
Made by Renesas Technology Corporation

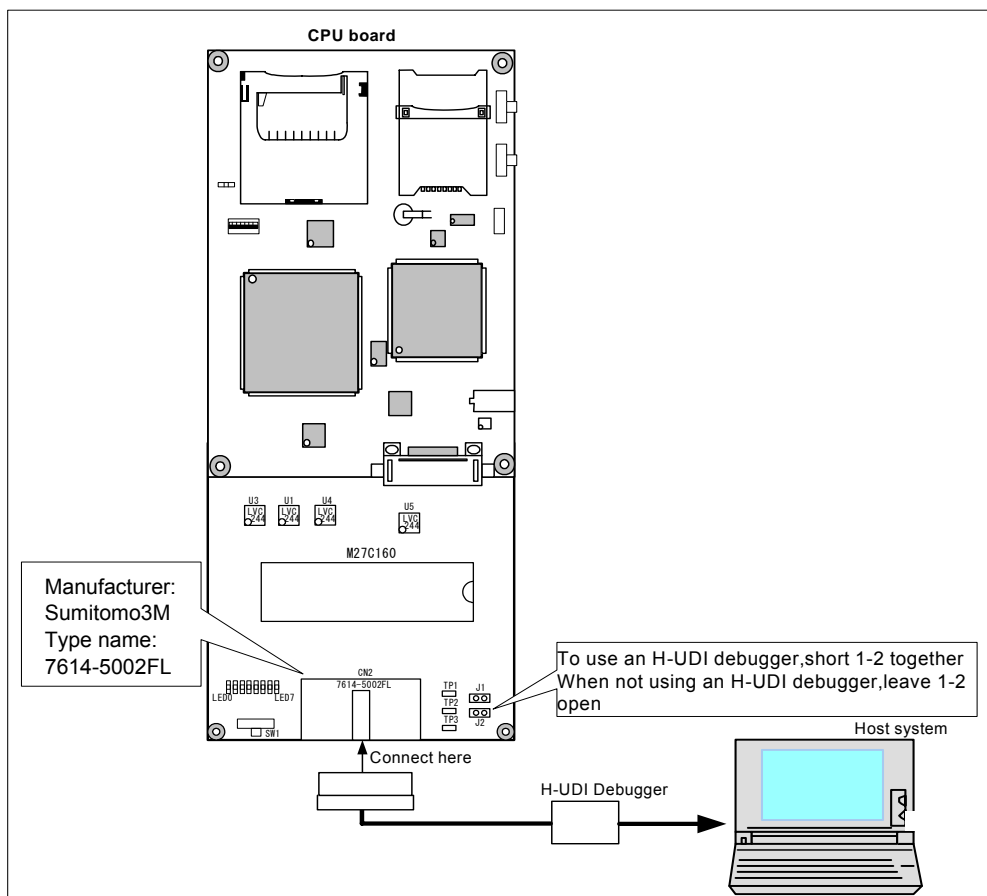


Figure 2.6 Connecting an H-UDI Debugger

[MEMO]

Chapter 3. Description of Switches

3.1 Switches on the CPU Board

Figure 3.1 shows switches SW1–SW3 mounted on the CPU board. The functions of switches SW1–SW3 are detailed in paragraphs (1) to (3) below.

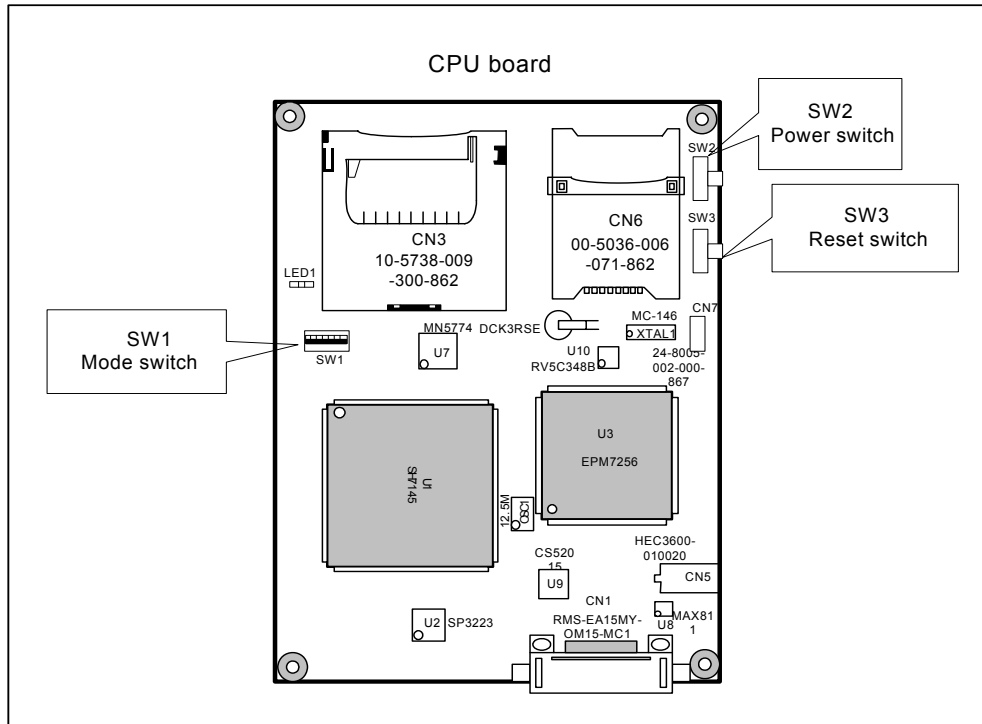


Figure 3.1 Switches SW1–SW3 on the CPU Board

(4) Power-on switch (SW2)

This switch turns on or off the power to the μ T-Engine board.

Holding down this switch for 0.5 seconds or more turns on the power to the μ T-Engine board. When you hold down this switch for 2 seconds or more while the power to the μ T-Engine board is on, the board is powered off.

(5) Reset switch (SW3)

This switch resets the μ T-Engine board.

Pressing this switch places the μ T-Engine board into a reset state, and when you release the switch, the μ T-Engine board is freed from the reset state and starts up.

(6) Mode switch (SW1)

Figure 3.2 shows how the 8-bit mode switch is set. Table 3.1 shows the relationship between modes and switch settings.

SW1 is a DIP switch used to set various startup modes of the μ T-Engine board.

(a) SW1-1 to 2 connect to mode pins of the SH7145.

For ON setting, the corresponding mode pins are set to the low level.

For OFF setting, the corresponding mode pins are set to the high level.

(b) SW1-3 connects to the FWP pin of the SH7145.

For ON setting, the FWP pin is set to the low level (= internal flash memory programming mode).

For OFF setting, the FWP pin is set to the high level (= normal mode). (Factory default)

(c) SW1-8 sets power-on conditions of the μ T-Engine board.

For ON setting, the power to the μ T-Engine board is turned on when it is supplied with power from the AC adapter. (Factory default)

For OFF setting, the power to the μ T-Engine board is turned on by pressing the power switch.

(d) SW1-3 to 7 connect to the input port of the SH7145 (PF4–7).

For ON setting, the corresponding input pins are set to the low level.

For OFF setting, the corresponding input pins are set to the high level. (Factory default)

Table 3.1 Mode Settings

Mode No.	SW1-1 (MD0)	SW1-2 (MD1)	Mode name	Internal ROM	Bus width	Remark
Mode 0	0	0	MCU extension mode 0	Disable	16bit	
Mode 1	1	0	MCU extension mode 1	-	-	Settings prohibited
Mode 2	0	1	MCU extension mode 2	Enable	Set by BCR1	(Factory default)
Mode 3	1	1	Single-chip mode	-	-	Settings prohibited

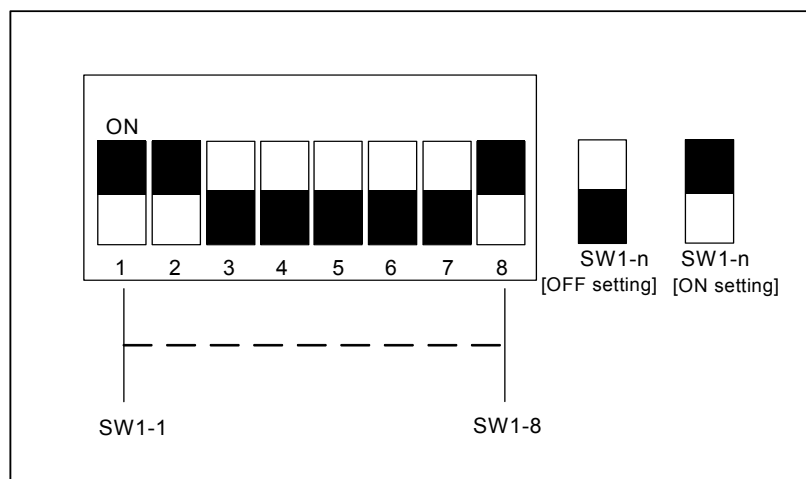


Figure 3.2 Settings of the 8-bit DIP Switch

Chapter 4. Memory Map

4.1 Memory Map for the Single μ T-Engine Board Case

Table 4.1 shows a memory map of the SH7145 when the CPU board only is connected in the system, with CPU operation mode 0 selected.

Table 4.2 shows a memory map of the SH7145 when the CPU board only is connected in the system, with CPU operation mode 2 selected. In this case, all CS spaces except CS0 are the same as in Table 4.1.

Table 4.1 SH7145 Memory Map for the Single μ T-Engine Board Case (MD = 0))

CS space	Bus width	Address	Device	Remark
CS0 space	16bit	h'00000000 -- h'000FFFFFFF	Flash Memory 1MB MBM29LV800TA70PBT(Fujitsu) \times 1	Software wait =3 External wait =0 Idle cycle =1
		h'00100000 -- h'002FFFFFFF	—	
		h'00300000 -- h'003FFFFFFF	SRAM 1MB TC55VEM316AXBN55 (Toshiba) \times 1	
CS1 space	16bit	h'00400000 -- h'004000FF	SD Card I/F controller MN5774(Matsushita)	Software wait =3 External wait = variable Idle cycle =1
		h'00400100 -- h'007FFFFFFF	Image	
CS2 space	16bit	h'00800000 -- h'00BFFFFFFF	CF Card I/F controller MR-SHPC-01 V2T(Marubun)	Software wait =5 External wait = variable Idle cycle =1
CS3 space	16bit	h'00C00000 -- h'00FFFFFFF	Extension bus I/F	Software wait = arbitrary External wait = arbitrary Idle cycle = arbitrary
Reserved	—	h'01000000 -- h'FFFFFF7FFF	—	
Peripheral I/O	—	h'FFFFFF8000 -- h'FFFFFFBFFF	—	
Reserved	—	h'FFFFFFC000 -- h'FFFFFFDFFF	—	
Internal RAM	—	h'FFFFFFE000 -- h'FFFFFFF	Internal RAM 8kB	

Table 4.2 SH7145 Memory Map for the Single μ T-Engine Board Case (MD = 2)

CS space	Bus width	Address	Device	Remark
Internal ROM		h'00000000 -- h'0003FFFF	Internal Flash Memory 256kB	
Reserved	—	h'00040000 -- h'001FFFFFFF	—	
CS0 space	16bit	h'00200000 -- h'002FFFFFFF	Flash Memory 1MB MBM29LV800TA70PBT(Fujitsu) \times 1	Software wait =3 External wait =0 Idle cycle =1
		h'00300000 -- h'003FFFFFFF	SRAM 1MB TC55VEM316AXBN55 (Toshiba) \times 1	

4.2 Memory Map for the Debug Board Connected Case

Table 4.3 shows a memory map of the SH7145 when CPU operation mode 0 (internal ROM disabled) is selected and the CPU board has a debug board connected to it, with J1 on the debug board left open. Table 4.4 shows a memory map of the SH7145 for the same case as described above, except that J1 on the debug board is shorted.

Table 4.5 shows a memory map of the SH7145 when CPU operation mode 2 (internal ROM enabled) is selected and the CPU board has a debug board connected to it. Note that when the internal ROM is enabled, the EPROM is always disabled no matter how J1 on the debug board is set.

Note also that all CS spaces except CS0 are the same as in Table 4.1.

Table 4.3 Memory Map for the Debug Board Connected Case (J1: Open, MD = 0)

CS space	Bus width	Address	Device	Remark
CS0 SPACE	16bit	h'00000000	Flash Memory	Software wait =3 External wait =0 Idle cycle =1
		--	1MB	
		h'000FFFFFFF	MBM29LV800TA70PBT(Fujitsu)×1	
		h'00100000	EPROM	
		--	2MB	
h'002FFFFFFF	M27C160-50F1(ST Micro)×1			
h'00300000	SRAM			
--	1MB			
h'003FFFFFFF	TC55VEM316AXBN55 (Toshiba)×1			

Table 4.4 Memory Map for the Debug Board Connected Case (J1: Shorted, MD = 0)

CS space	Bus width	Address	Device	Remark
CS0 SPACE	16bit	h'00000000	EPROM	Software wait =3 External wait =0 Idle cycle =1
		--	2MB	
		h'001FFFFFFF	M27C160-50F1(ST Micro)×1	
		h'00200000	Flash Memory	
		--	1MB	
		h'002FFFFFFF	MBM29LV800TA70PBT(Fujitsu)×1	
h'00300000	SRAM			
--	1MB			
h'003FFFFFFF	TC55VEM316AXBN55 (Toshiba)×1			

Table 4.5 Memory Map for the Debug Board Connected Case (J1: Open, MD = 2)

CS space	Bus width	Address	Device	Remark
Internal ROM	--	h'00000000	Internal Flash Memory	
		--	256kB	
Reserved	--	h'00040000		
		--		
		h'001FFFFFFF		
CS0 SPACE	16bit	h'00200000	Flash Memory	Software wait =3 External wait =0 Idle cycle =1
		--	1MB	
		h'002FFFFFFF	MBM29LV800TA70PBT(Fujitsu)×1	
		h'00300000	SRAM	
		--	1MB	
h'003FFFFFFF	TC55VEM316AXBN55 (Toshiba)×1			

Chapter 5. Functional Blocks

5.1 CF Card Interface

5.1.1 Description of the Block

Figure 5.1 shows the CF card control block of the μ T-Engine board. As shown in Figure 5.1, the CF card control block incorporates a controller (MR-SHPC-01 V2 made by Marubun), a 50-pin PC card interface connector (CN2), and a power supply control IC (TPS2211DB made by TI). The controller interfaces with PC Card Standard 97-compliant cards. Its features are outlined below.

- (1) Incorporates two memory window boards and one I/O window board
- (2) Incorporates a card access timing adjustment function
- (3) Incorporates a read/write buffer comprised of one stag
- (4) Incorporates an endian control circuit
- (5) Supports 5.0V/3.3V cards
- (6) Does not require external buffers
- (7) Incorporates an interrupt steering function
- (8) Incorporates a power-down function
- (9) Incorporates a suspend function

The controller interrupts ($_SIRQ3$ to $_SIRQ0$) are AND'ed in the CPLD before being input to $_IRQ2$ of the SH7145.

For more information, refer to the user's manual for the MR-SHPC-01 V2 made by Marubun.

Marubun web site <http://www.marubun.co.jp/>

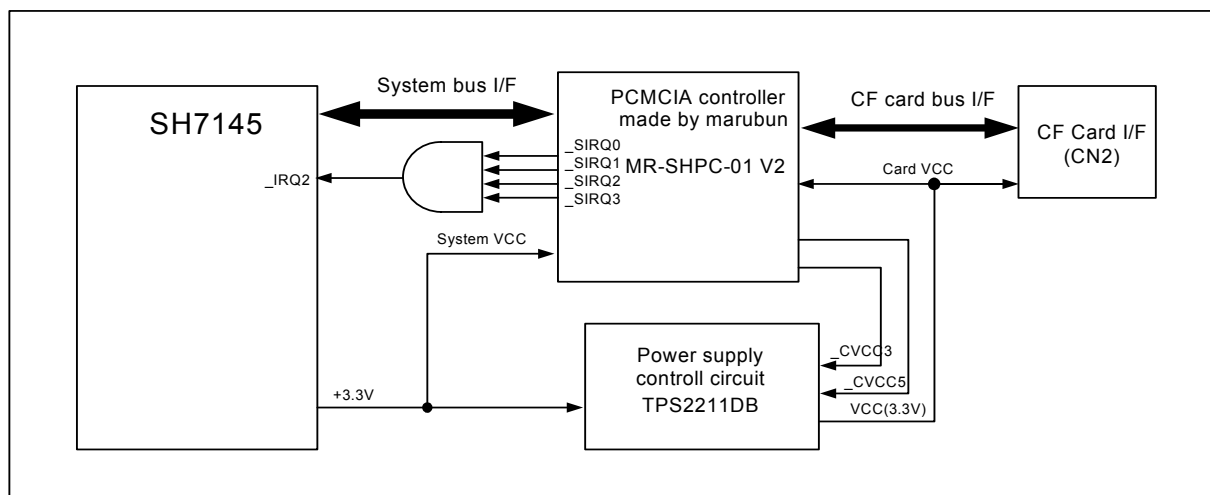


Figure 5.1 CF Card Control Block

CAUTION



Only the 3.3 V type of CF card can be connected.

5.1.2 Connector Pin Arrangement

Table 5.1 lists the pin arrangement of the 50-pin CF card interface connector (CN2).

Table 5.1 Signal Assignments of the CF Card Interface Connector

Pin	Memory card			I/O card		
	Signal	I/O	Function	Signal	I/O	Function
1	GND	—	Ground	GND	—	Ground
2	D3	I/O	Data bit3	D3	I/O	Data bit3
3	D4	I/O	Data bit4	D4	I/O	Data bit4
4	D5	I/O	Data bit5	D5	I/O	Data bit5
5	D6	I/O	Data bit6	D6	I/O	Data bit6
6	D7	I/O	Data bit7	D7	I/O	Data bit7
7	CE1#	O	Card enable	CE1#	O	Card enable
8	A10	O	Address bit10	A10	O	Address bit10
9	OE#	O	Output enable	OE#	O	Output enable
10	A9	O	Address bit9	A9	O	Address bit9
11	A8	O	Address bit8	A8	O	Address bit8
12	A7	O	Address bit7	A7	O	Address bit7
13	Vcc	-	Power supply	Vcc	-	Power supply
14	A6	O	Address bit6	A6	O	Address bit6
15	A5	O	Address bit5	A5	O	Address bit5
16	A4	O	Address bit4	A4	O	Address bit4
17	A3	O	Address bit3	A3	O	Address bit3
18	A2	O	Address bit2	A2	O	Address bit2
19	A1	O	Address bit1	A1	O	Address bit1
20	A0	O	Address bit0	A0	O	Address bit0
21	D0	I/O	Data bit0	D0	I/O	Data bit0
22	D1	I/O	Data bit1	D1	I/O	Data bit1
23	D2	I/O	Data bit2	D2	I/O	Data bit2
24	WP	I	Write protect	IOIS16#	I	16bit I/O port
25	CD2#	I	Card detection	CD2#	I	Card detection
26	CD1#	I	Card detection	CD1#	I	Card detection
27	D11	I/O	Data bit11	D11	I/O	Data bit11
28	D12	I/O	Data bit12	D12	I/O	Data bit12
29	D13	I/O	Data bit13	D13	I/O	Data bit13
30	D14	I/O	Data bit14	D14	I/O	Data bit14
31	D15	I/O	Data bit15	D15	I/O	Data bit15
32	CE2#	O	Card enable	CE2#	O	Card enable
33	VS1	I	Voltage sense	VS1	I	Voltage sense
34	IORD#	I	I/O read	IORD#	I	I/O read
35	IOWR#	O	I/O write	IOWR#	O	I/O write
36	WE#	O	Write enable	WE#	O	Write enable
37	READY	I	Ready	READY	I	Ready
38	Vcc	-	Power supply	Vcc	-	Power supply
39	CSEL#	O	Card select	CSEL#	O	Card select
40	VS2#	I	Voltage sense	VS2#	I	Voltage sense
41	RESET	O	Card reset	RESET	O	Card reset
42	WAIT#	I	Bus cycle extension	WAIT#	I	Bus cycle extension
43	INPACK#	I	Input port response	INPACK#	I	Input port response
44	REG#	O	Register select	REG#	O	Register select
45	BVD2	I/O	Battery voltage detection	SPKR#	I/O	Audio digital waveform
46	BVD1	I/O	Battery voltage detection	STSCHG#	I/O	Card status change
47	D8	I/O	Data bit8	D8	I/O	Data bit8
48	D9	I/O	Data bit9	D9	I/O	Data bit9
49	D10	I/O	Data bit10	D10	I/O	Data bit10
50	GND	-	Ground	GND	-	Ground

5.1.3 Register Map

Table 5.2 shows a register map of the CF card controller. All registers should be accessed wordwise.

Table 5.2 CF Card Controller Register Map

Address	Initial value	Register name
H'B83FFFE4	H'0000	Mode register
H'B83FFFE6	H'000C	Option register
H'B83FFFE8	H'03BF	Card status register
H'B83FFFEA	H'0000	Interrupt source register
H'B83FFFE C	H'0000	Interrupt control register
H'B83FFFE E	H'0000	Card power supply control register
H'B83FFF0	H'07FC	Memory window 0 control register 1
H'B83FFF2	H'07FC	Memory window 1 control register 1
H'B83FFF4	H'07FC	I/O window control register
H'B83FFF6	H'0000	Memory window 0 control register 2
H'B83FFF8	H'0000	Memory window 1 control register 2
H'B83FFFA	H'0000	I/O window control register
H'B83FFFC	H'0000	Card control register
H'B83FFFE	H'5333	Chip information register

5.2 Serial Interface

5.2.1 Description of the Block

Figure 5.2 shows the UART control block of the μ T-Engine board. As shown in Figure 5.2, it consists of the internal serial controller of the SH7145, an RS-232C interface driver, and a 15-pin serial connector (CN1), so that this control block can be used as a debug interface when it is connected to a PC at the RS-232C level via the 15-pin serial connector (CN1). Transfers between this block and the PC are timed with respect to the peripheral clock of the SH7145.

For more information, refer to the user's manual of the SH7145.

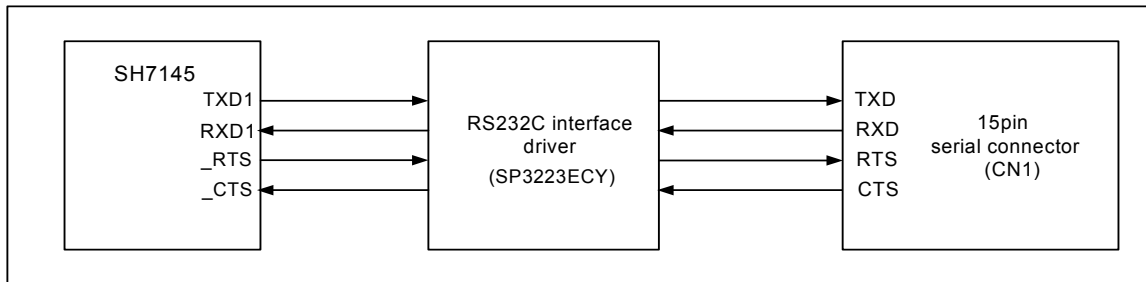


Figure 5.2 Serial Interface Control Block

5.2.2 Connector Pin Arrangement

Table 5.3 shows the pin arrangement of the 15-pin serial connector (CN1).

Table 5.3 Pin Arrangement of the Serial Interface Host Connector (CN1)

Pin No	Signal	I/O	Remark
1	GND	—	
2	TxD	O	SCI1
3	RxD	I	SCI1
4	GND	—	
5	RTS	O	CPU PA8
6	CTS	I	CPU PA9
7	GND	—	
8	Reserved	—	ISP TCK
9	Reserved	—	GND
10	Reserved	—	ISP TMS
11	Reserved	—	NC(ISP Plug)
12	Reserved	—	NC(ISP BScan)
13	Reserved	—	ISP TDI
14	Reserved	—	ISP TDO
15	Reserved	—	Vcc(3.3V)

5.2.3 Register Map

Table 5.4 shows a register map of the serial controller (SCI1).

Table 5.4 Serial Controller Register Map (SCI1)

Name	Abbreviation	R/W	Initial value	Address	Access size
Serial mode register_1	SMR_1	R/W	H'00	H'FFFF81B0	8
Bit rate register_1	BRR_1	R/W	H'FF	H'FFFF81B1	8
Serial control register_1	SCR_1	R/W	H'00	H'FFFF81B2	8
Transmit data register_1	TDR_1	R/W	H'FF	H'FFFF81B3	8
Serial status register_1	SSR_1	R/W	H'84	H'FFFF81B4	8
Receive data register_1	RDR_1	R	H'00	H'FFFF81B5	8
Serial direction control register_1	SDCR_1	R/W	H'F2	H'FFFF81B6	8

5.3 SD Card Interface

The controller used in the μ T-Engine board for SD card interface is the MN5774 made by Matsushita.

5.3.1 Connector Pin Arrangement

Table 5.5 shows the pin arrangement of the 12-pin SD card interface connector (CN3).

Table 5.5 Pin Arrangement of the SD Card Interface Connector (CN3)

Pin №	Signal name	I/O	Remark
1	SD_CD/SD_DAT3	I/O	
2	SD_CMD	I/O	
3	VSS	—	
4	VDD	—	Can be turned on/off
5	SD_CLK	O	
6	VSS	—	
7	SD_DAT0	I/O	
8	SD_DAT1	I/O	
9	SD_DAT2	I/O	
10	SD_CP	I	(SD_WP)
11	SD_CD	I	
12	COM	—	Connects to GND

5.3.2 Register Map

The registers of the SD controller are mapped to memory beginning with the address H'00400000. All registers should be accessed wordwise.

5.4 eTRON Interface

5.4.1 Description of the Block

Figure 5.3 shows the eTRON interface control block of the μ T-Engine board. As shown in Figure 5.3, by using the serial interface controller (SCI0) of the SH7145, it is possible to communicate with an eTRON card inserted in the eTRON card interface connector (CN6).

The eTRON card can be reset or placed out of reset by controlling the port (PA23) of the SH7145, as described below.

Driving PA23 low causes the reset pin of the eTRON card to go low (reset state).

Driving PA23 high causes the reset pin of the eTRON card to go high (normal state).

The eTRON card is always supplied with power when the power to the μ T-Engine board is on. Always make sure the power to the μ T-Engine board is turned off before inserting or removing an eTRON card.

For more information, refer to the user's manual of the SH7145.

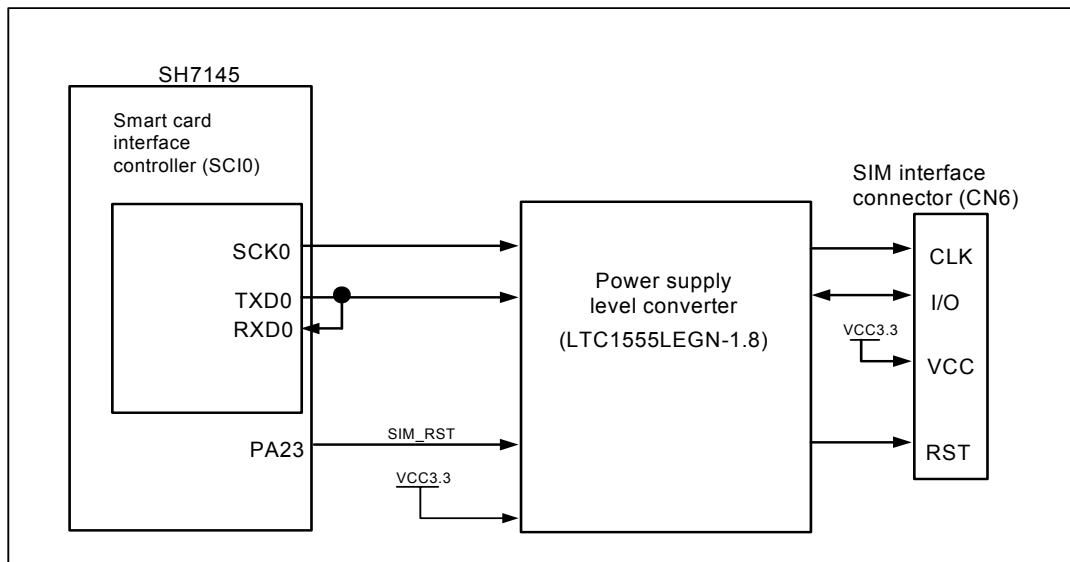


Figure 5.3 eTRON Interface Control Block

5.4.2 Connector Pin Arrangement

Figure 5.4 shows the pin arrangement of the eTRON card interface connector (CN6). Table 5.6 lists signal assignments of the eTRON card interface connector (CN6).

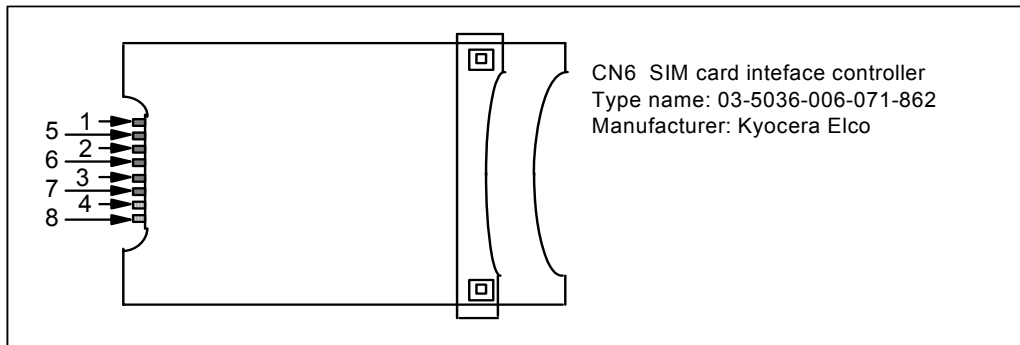


Figure 5.4 Pin Arrangement of the eTRON Interface Connector (CN6)

Table 5.6 Signal Assignments of the eTRON Interface Connector (CN6)

Pin No	Signal name
1	C1:VCC
2	C2:RST
3	C3:CLK
4	C4:□1
5	C5:GND
6	C6:VPP
7	C7:I/O
8	C8:□1

*1 Do not use pin Nos. 4 and 8 because they are connected to the board-testing connector (CN8).

5.4.3 Register Map

Table 5.7 shows a register map of the internal serial interface controller (SCI0) of the SH7145.

Table 5.7 Serial Interface Register Map

Name	Abbreviation	R/W	Initial value	Address	Access size
Serial mode register_0	SMR_0	R/W	H'00	H'FFFF81A0	8
Bit rate register_0	BRR_0	R/W	H'FF	H'FFFF81A1	8
Serial control register_0	SCR_0	R/W	H'00	H'FFFF81A2	8
Transmit data register_0	TDR_0	R/W	H'FF	H'FFFF81A3	8
Serial status register_0	SSR_0	R/W	H'84	H'FFFF81A4	8
Receive data register_0	RDR_0	R	H'00	H'FFFF81A5	8
Serial direction control register_0	SDCR_0	R/W	H'F2	H'FFFF81A6	8

[MEMO]

Chapter 6. External Interrupts

6.1 External Interrupts of the SH7145

Figure 6.1 shows a configuration of the interrupt signals of the SH7145.

Table 6.1 shows the relationship between interrupt sources and interrupt signals.

As shown in Figure 6.1, the interrupt signals from the respective devices of the μ T-Engine board are connected to the `_IRQ0` through `_IRQ2` pins of the SH7145. The interrupt signal from the expansion slot is connected to `_IRQ3`.

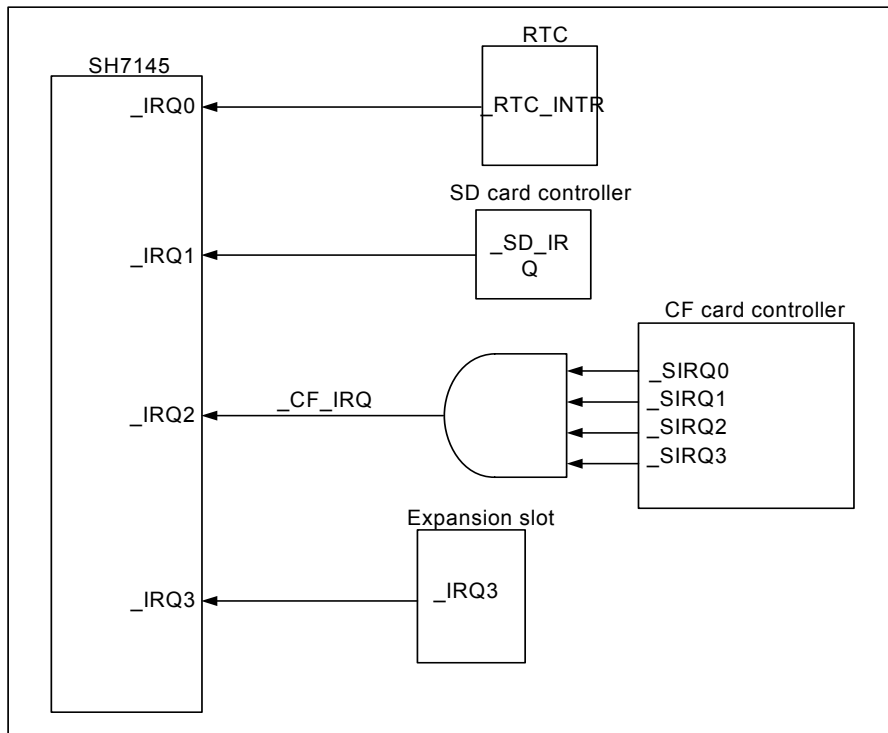


Figure 6.1 Configuration of Interrupt Signals

Table 6.1 Relationship between Interrupt Sources and Interrupt Signals

No.	Interrupt requesting source	Interrupt input pin	Interrupt signal level	Remark
1	RTC controller	<code>_IRQ0</code>	Active Low	
2	SD card controller	<code>_IRQ1</code>	Active Low	
3	PCMCIA controller	<code>_IRQ2</code>	Active Low	
4	Expansion slot/IRQ3	<code>_IRQ3</code>	Active Low	

[MEMO]

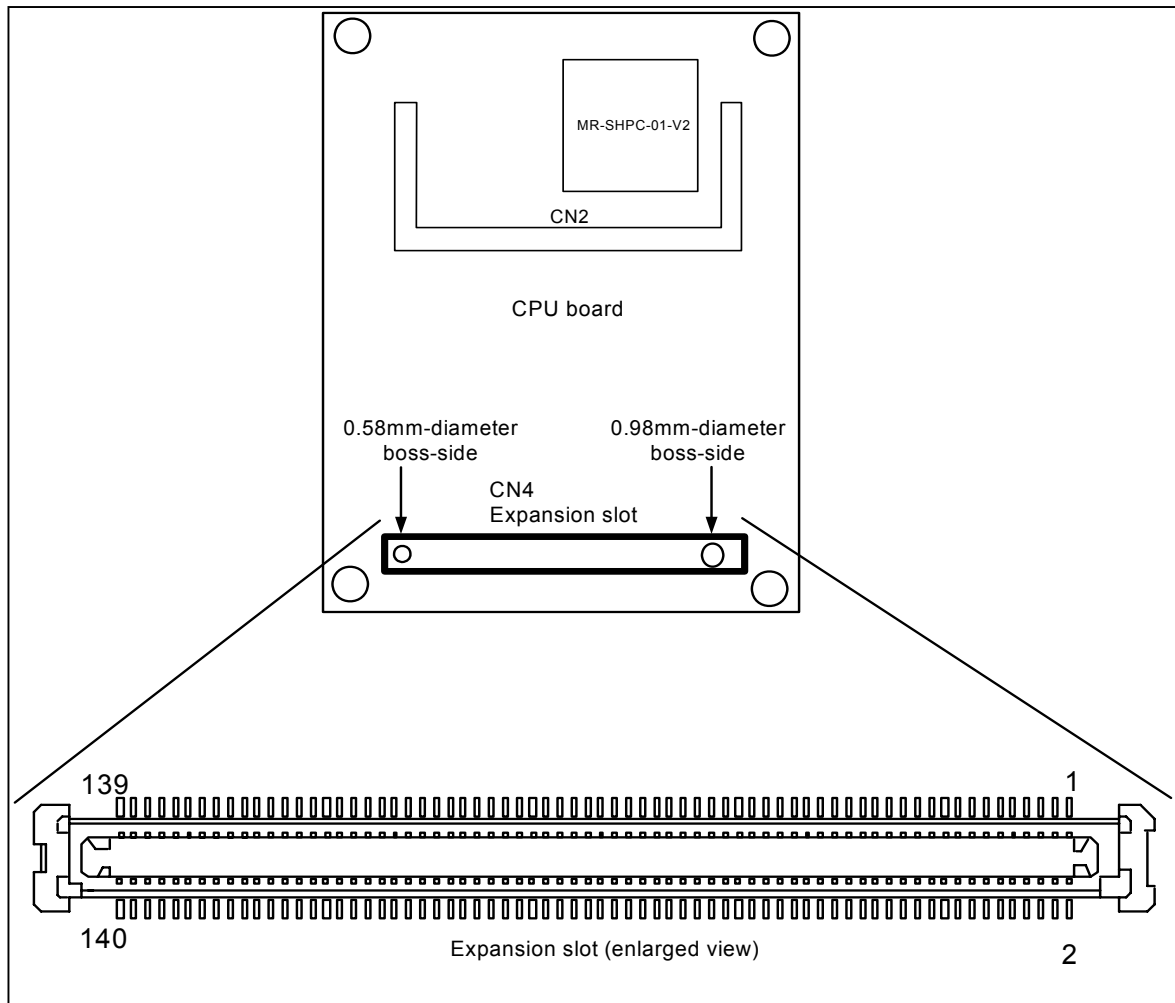
Chapter 7. μ T-Engine Board Expansion Slot

7.1 Specifications of the Expansion Slot

Figure 7.1 shows the arrangement of the expansion slot on the CPU board.

- Connector number: CN4
- Connector type mounted on the μ T-Engine board: 20-5603-14-0102-861 (Kyocera Elco)
- Compatible connector type: 10-5603-14-0102-861 (Kyocera Elco)

Figure 7.1 Expansion Slot Signal Assignments



7.2 Expansion Slot Signal Assignments

Table 7.1 lists signal assignments of the expansion slot.

Table 7.1 Expansion Slot Signal Assignments

Pin No.	Signal name	I/O	Pin No.	Signal name	I/O	Pin No.	Signal name	I/O	Pin No.	Signal name	I/O
1	-	-	36	PD29	O	71	-	-	106	-	-
2	-	-	37	PD30	O	72	-	-	107	-	-
3	-	-	38	PD31	O	73	EPROMCE	O	108	DBGMD	I
4	-	-	39	GND	-	74	CS3	O	109	GND	-
5	D0	I/O	40	GND	-	75	-	-	110	GND	-
6	D1	I/O	41	CK	O	76	PE13/TIOC4B	O	111	TCK	I
7	D2	I/O	42	GND	-	77	PE14/TIOC4C	O	112	TMS	I
8	D3	I/O	43	GND	-	78	PE15/TIOC4D	O	113	TRST	I
9	D4	I/O	44	GND	-	79	GND	-	114	TDI	I
10	D5	I/O	45	A0	O	80	GND	-	115	TDO	O
11	D6	I/O	46	A1	O	81	RD	O	116	ASEBRKAK	O
12	D7	I/O	47	A2	O	82	WAIT	I	117	3.3VSB	-
13	D8	I/O	48	A3	O	83	WRL	O	118	3.3VSB	-
14	D9	I/O	49	A4	O	84	WRH	O	119	3.3VSB	-
15	D10	I/O	50	A5	O	85	-	-	120	3.3VSB	-
16	D11	I/O	51	A6	O	86	-	-	121	PE0/TIOC0A	O
17	D12	I/O	52	A7	O	87	GND	-	122	PE1/TIOC0B	O
18	D13	I/O	53	A8	O	88	GND	-	123	PE2/TIOC0C	O
19	D14	I/O	54	A9	O	89	-	-	124	PE3/TIOC0D	O
20	D15	I/O	55	A10	O	90	-	-	125	PE6/TIOC2A	O
21	GND	-	56	A11	O	91	-	-	126	-	-
22	GND	-	57	A12	O	92	IRQ3	I	127	3.3V	-
23	PD16	O	58	A13	O	93	NMI_IN	I	128	3.3V	-
24	PD17	O	59	A14	O	94	RES_IN	I	129	3.3V	-
25	PD18	O	60	A15	O	95	RES_OUT	O	130	3.3V	-
26	PD19	O	61	GND	-	96	-	-	131	3.3V	-
27	-	-	62	GND	-	97	-	-	132	3.3V	-
28	PD21	I/O	63	A16	O	98	-	-	133	VBAT_IN	-
29	CONT1	O	64	A17	O	99	ROMSEL	I	134	VBAT_IN	-
30	CONT2	O	65	A18	O	100	-	-	135	VBAT_IN	-
31	DREQ0	I	66	A19	O	101	GND	-	136	VBAT_IN	-
32	PD25	I/O	67	A20	O	102	GND	-	137	GND	-
33	DACK0	O	68	A21	O	103	SCI_TXD3	O	138	GND	-
34	PD27	I/O	69	-	-	104	SCI_RXD3	I	139	GND	-
35	PD28	O	70	-	-	105	-	-	140	GND	-

Chapter 8. Daughter Board Design Guide

This chapter describes how to design a daughter board, which will be connected to the μ T-Engine board via its expansion slot.

A daughter board refers to the board that can be controlled by the address bus, data bus, and control signals or serial interface of the SH7145 that are output to the expansion slot of the μ T-Engine board.

8.1 Board Size of the Daughter Board

The daughter board is recommended to be prepared in a size equal to that of the CPU board (85 mm x 60 mm) of the μ T-Engine board.

8.2 Power Supply to the Daughter Board

Table 8.1 lists the power supply voltage and current that can be supplied from the μ T-Engine board to the daughter board. If the permissible amount of current for the daughter board is exceeded, the daughter board must be provided with an appropriate means of power supply on it.

Table 8.1 Voltage and Current Suppliable to the Daughter Board

Expansion slot signal name	Output voltage	Permissible amount of current	Remark
3.3V 3.3VSB	3.3V	250mA	3.3V: Supplied when power for the SH7145 is on 3.3VSB: Always supplied when the AC adapter is connected

CAUTION



- The permissible amount of current for 3.3 V and 3.3 VSB in Table 8.1 is the sum total of 3.3 V and 3.3 VSB.
- If the μ T-Engine board has a CF card connected to it, the permissible amount of current stipulated above must be deducted by an amount equal to the amount of current consumed by the CF card. For example, if a 3.3 V / 100 mA power supply is used for the CF card, then the permissible amount of current for 3.3 V usable in the expansion slot is 250 mA – 100 mA = 150 mA. For details, refer to Table 1.3, "Permissible Amount of Current that Can Be Supplied to the Outside."

8.3 Daughter Board Stack

Up to two daughter boards can be connected to the μ T-Engine board in a stack.

When connecting more than one daughter board in a stack, pay attention to the power supply capacity available for the daughter boards.

Figure 8.1 shows an example configuration of a daughter board stack.

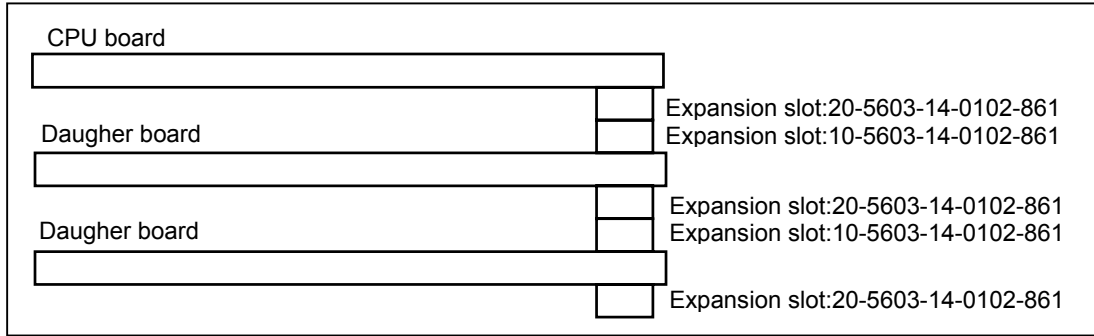


Figure 8.1 Configuration of a Daughter Board Stack

8.4 /WAIT Output of the Daughter Board

To accept /WAIT input from the daughter board, the μ T-Engine board has one /WAIT input pin provided in its expansion slot. To output /WAIT from the daughter board, use an open-collector arrangement in order to prevent collision of /WAIT outputs in cases when two daughter boards are connected in a stack.

Note that the /WAIT pin on the μ T-Engine board side is pulled up to 3.3 V through 680 ohm. Figure 8.2 shows a configuration of the /WAIT pin of the expansion slot.

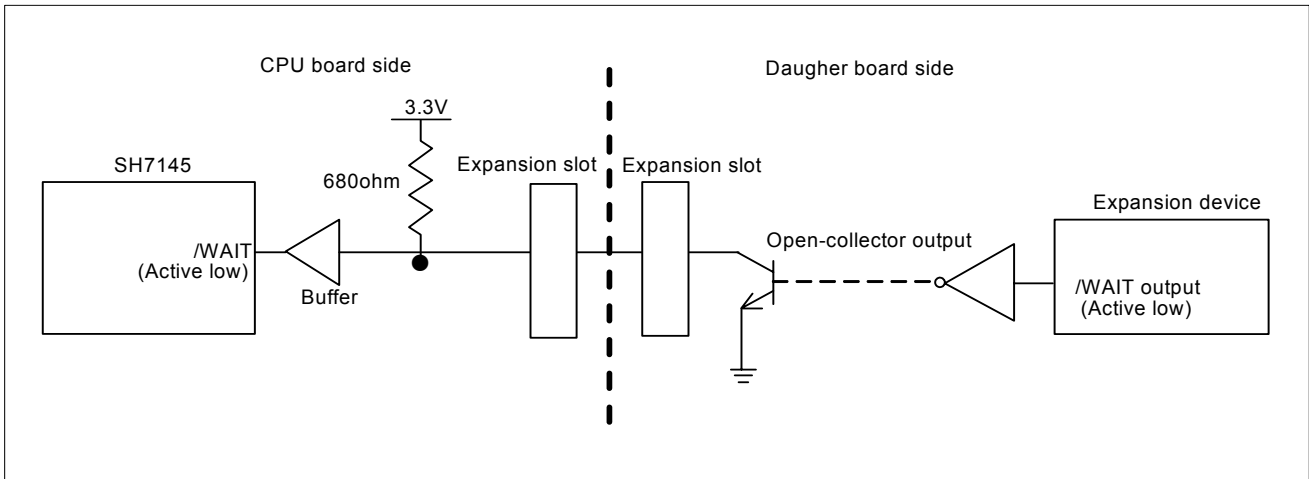


Figure 8.2 Configuration of the /WAIT Pin of the Expansion Slot

Chapter 9. Flash Memory Rewriting

Connect the debug board to the expansion slot (CN4) of the μ T-Engine board and run the program written into the EPROM on the debug board. That way, the flash memory in the μ T-Engine board can be rewritten.

9.1 Programming Preparation

Connect the debug board to the expansion slot (CN4) of the μ T-Engine board. Furthermore, set the jumper switch on the debug board as described below. For details, refer to Section 2.4.2, “Connecting the Debug Board,” and Section 2.4.3, “Jumper Switches on the Debug Board.”

Debug board jumper switch 1 (J1): 1–2 shorted (EPROM mapped to addresses h'00000000 through h'0001FFFF)

Debug board jumper switch 2 (J2): 1–2 open (SH7145 in normal operation mode)

Connect the μ T-Engine board and the host system by plugging the attached RS-232C interface cable into the serial interface connector (CN1) on the μ T-Engine board. Launch the communication software in the host system and set serial communication parameters as shown below.

Baud rate: 38400 bps

Data length: 8 bits

Parity bit: None

Stop bit: 1 bit

Flow control: Xon/Xoff

After the above settings are made, turn on the power to the μ T-Engine board. The title screen of the communication software showing the execution status of the internal program of the EPROM will be displayed, as shown below. The X.X on the displayed screen indicates the debugger version.

[Display screen]

```
=====
SH7145 Self Debugger VerX.X
=====
H[elp] for help messages...
Ready>
```

9.2 Rewriting the Flash Memory

Figure 9.1 shows an image depicting how the flash memory in the μ T-Engine board will be rewritten. As shown in Figure 9.1, rewriting of the internal flash memory of the μ T-Engine board is accomplished by first copying all data from the flash memory into the SRAM and then overwriting the SRAM with the data transferred from the host system and writing that data from the SRAM back to the flash memory.

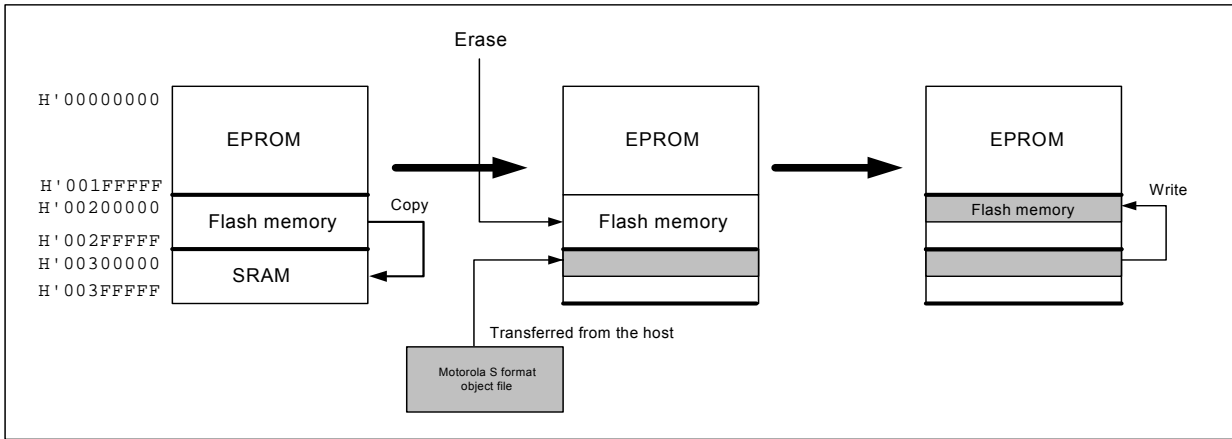


Figure 9.1 Flash Memory Rewrite Image

The following shows the procedure for rewriting the internal flash memory of the μ T-Engine board.

- (1) After the title screen of the communication software is displayed, enter "FL 0" and hit Enter as shown below.

[Display screen]

```
=====
SH7145 Self Debugger Ver X.X
=====
H[elp] for help messages...
Ready >fl 0 00200000
```

- (2) When a transfer request message “Please Send A S-format Record” is displayed as shown below, transfer a Motorola S-format object file.

```
[Display screen]
Ready >fl 0 00200000
FlashROM Data Copy To SRAM
Please Send A S-format Record
```

- (3) When the flash memory has been erased and programmed with new data after the Motorola S-format object file was transferred to it, a message “Flash write complete” similar to the one shown below will be displayed, indicating that the operation has finished normally.

CAUTION



While the host is rewriting the flash memory, never turn off the power to the μ T-Engine board. Data may not be written to correctly, or the flash memory may be damaged.

```
[Display screen]
Ready >fl 0 00200000
FlashROM Data Copy To SRAM
Please Send A S-format Record
Chip erase : complete
Program : complete
flash write complete
Ready >
```

[MEMO]

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